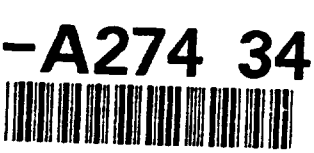

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Interim Technical Report:

Ferroelectric Fluoride Memory FET Development

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WESTINGHOUSE ELECTRIC CORPORATION
ELECTRONIC SYSTEMS GROUP
BALTIMORE, MARYLAND 21203

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FOR INTEGRATED ELECTRONICS

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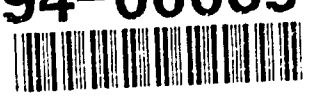

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This Interim Technical Report covers the development and integration of Barium Magnesium Fluoride (BMF) ferroelectric thin films for incorporation into the gate dielectric of a metal-insulator-silicon field effect transistor, capable of functioning in a non-volatile, nondestructive-readout (NDRO) ferroelectric random access memory (FERRAM). Also provided is a detailed description of the test vehicles implemented for the study of fabrication process integration and optimization and the resultant properties of "ferroelectric/(semiconductor) memory FET (FEMFET) and related structures". The BMF films were deposited by co-evaporation in ultra high vacuum from barium fluoride and magnesium fluoride effusion sources. A substrate temperature of 200°C during deposition followed by an anneal in hydrogen at 480°C

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resulted in polarization orientation closest to the preferred. Film samples exhibited polarization, Ps, as high as 4.55μC/cm^2. The permitivity varied from a value of 9 at 5 kHz to 8.4 at 500 kHz. This compares closely with the average value of 10 reported for bulk single crystals. The ferroelectric switching speed of the thin film was approximately 45 nanoseconds.

Ferroelectric measurements with a RT-66A test system showed only a 22% reduction in remanent polarization after 2.9 x 10^9 switching cycles at 60V, and polarization retention experiments showed a polarization change rate exceeding 2.75nC/cm^2/"time decade" during a nearly 10 days period. That charge drift converts directly into FEMFET threshold drift which causes closure of the nonvolatile NDRO memory window. Retention times for a number of BMF dielectric FEMFETs ranged from 1 to 5 hours. Using capacitance-voltage (CV) techniques, measurements of ferroelectric BMF test capacitors, as a function of time after positive and negative programming, were correlated with CV hysteresis data; and imputed memory window decay rates (per "decade of time") were calculated. Those imputed retention times were also in the range of hours like the retention measured on the BMF FEMFETs. Temperature-bias stress measurements on these capacitors indicated that mobile charges were a significant factor in producing such fast decay rates for the memory window. Ionic conductivity of BMF, especially noticeable above 25°C, strongly influences FEMFET retention. Indeed this was an important factor in the decision to shift the focus of this experimental FEMFET development program from BMF to other ferroelectric materials.

The coauthors of this report wish to acknowledge experimental and developmental contributions from Mary Austin, Murray Polinsky, Paul Brabant and Ed Stepke at Westinghouse, consulting and specialized measurements from Dr. S.B. Krupanidhi (Penn State) and Dr. Seshu Desu (VPI), as well as advice and consulting from Drs. Don Smyth and Marvin White (Lehigh), and Dr. S.Y. Wu (McDonnell-Douglas).

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1.0 EXECUTIVE SUMMARY

The Westinghouse contract is aimed towards the development of a 4-inch silicon wafer technology for FERRAM/FEMFET (Ferroelectric Memory FET) memory arrays. The memory cell structure involves a ferroelectric layer within the gate dielectric of the FET, where the ferroelectric may be a ferroelectric fluoride (BMF) or some other ferroelectric like bismuth titanate, $Bi_4Ti_3O_{12}$. The key aspects of the program address (a) development of Integration Compatibility/Accelerated Lifetime (ICAL) test vehicles (including prototype FEMFET structures), (b) optimization of the ferroelectric fluoride or oxide films as low-coercivity dielectrics, (c) evaluation of aging and fatigue effects and demonstration of long-term device stability in optimized transistor structures, and (d) development of large-area manufacturing process compatible with a 4-inch FERRAM/FEMFET technology.

This Interim Report covers the development of the barium magnesium fluoride (denoted as BMF) memory FET and a detailed description of the ICAL test vehicle implemented for the study of ferroelectric/semiconductor structures properties and FEMFET fabrication process development and optimization.

A strong positive attribute of BMF for use in FEMFET device structures is its chemical compatibility with silicon. Initial studies demonstrating the UHV deposition of BMF on clean silicon surfaces resulted in very low interface state densities. It was also found that relatively large memory threshold voltage windows could be obtained in MIS structures with modest values of switched polarization. Therefore, it was felt that transistor structures exhibiting high performance FERRAM-FEMFET operation could be achieved by incorporating UHV-deposited ferroelectric BMF films as the gate dielectric on silicon substrates. The study approach was to vary systematically the growth and annealing conditions and through correlative analysis and electrical CV measurements to establish BMF fabrication procedures suitable for construction of high-performance and stable FEMFET memory cells and arrays.

Epitaxial conditions where the ferroelectric a-axis of the BMF lies perpendicular to the film plane were not identified. Thus to obtain significant ferroelectric switching it was necessary to utilize samples which are randomly oriented. It was found that films grown at 200°C and annealed in hydrogen at 480°C resulted in an almost perfect random orientation. Electrical measurements on capacitor structures confirmed that much higher values of switched polarization were obtained from more randomly oriented BMF films. For the best film samples the value of P_S measured has been as high as 4.55 $\mu C/cm^2$. Dielectric permittivity and dissipation factor were measured over a frequency range of 5 to 500 kHz. The permittivity displayed some variation with frequency, falling from a value of 9 at 5 kHz to 8.4 at 500 kHz. This compares closely with the average value of 10 reported for bulk single crystals. This low value of permittivity provides a significant advantage compared to oxide ferroelectrics.

In general, SiO_2-capped BMF films with aluminum dot top electrodes exhibited CV memory windows that exceeded the programming voltage. For instance, a 21V memory window was obtained with 16V programming. The ferroelectric switching speed for BMF films was measured at Penn State University to be in the range of 40 to 45 nanoseconds. Fatigue measurements made using an RT-66A test system showed only a 22% reduction in the remanent polarization (P^*_r) after 2.9×10^9 switching cycles at 60V. Retention

experiments with the RT-66A test system showed polarization decay rate of 2.75nCoulombs/cm^2/(time decade) from one minute to over 1000 minutes for the linear regression best fit for that time region.

An 8K FERRAM Test Vehicle was created for evaluation of FEMFET baseline process integrity. This mask set featured a full complement of test structures for evaluation of the process integrity of the FEMFET process. These test structures address such issues as performance, reliability, producibility, radiation hardness, and uniformity of the baseline technology. Wafer fabrication on this program used short-loop gridded wafers for ferroelectric capacitor fabrication and fully processed device wafers for FEMFET fabrication. During this program phase 150 gridded wafers were processed and 20 device wafers were processed up to FEMFET formation.

Process optimization for such parameters as buffer oxide thickness, ferroelectric film thickness/growth ambient, capping oxide, film anneal, and metal composition/thickness was performed on the short-loop gridded capacitor wafers. Upon successful demonstration of ferroelectric CV behavior, FEMFET memory transistors were fabricated. A total of 14 device wafers with BMF FEMFETs were obtained. A series of measurements were performed to quantify the retention characteristics of the BMF FEMFETs. In general, all of these evaluations indicated that the BMF FEMFETs that were fabricated had typical retention times of 1 to 5 hours.

Evaluation of gridded test capacitors by CV techniques included variation of capacitance with time after positive or negative write voltages. The variation of capacitance was correlated with CV curve data and imputed decay rate of memory window per decade of time was calculated. These rates for BMF, in general, agreed with the transistor measurements of retention of 1 to 5 hours. Also, several of the capacitor samples were temperature-bias stressed and the shift of CV curves noted. These retention and temperature-bias stress tests indicated that mobile charges were a significant factor in producing a fast decay rate of the memory window. On the other hand the measurements on BMF films using the RT-66A test system showed that the ferroelectric spontaneous polarization, P_S, behaved well with endurance cycling and retention. Ionic conductivity of BMF, especially when the temperature is increased above 25°C was another factor that was considered and was a major point in deciding to shift the study of ferroelectric FEMFETs from BMF to other "oxide" ferroelectric materials such as bismuth titanate.

2.0 INTRODUCTION

The concept of a thin film ferroelectric memory field-effect transistor (FEMFET) is not new. The first FEMFET was demonstrated by S. Y. Wu[1] in 1974. The structure of that device was identical to the standard silicon metal-insulator-semiconductor field-effect transistor (MISFET), except that the insulator in the MISFET was replaced by a thin (3 to 4 μm) layer of sputter-deposited ferroelectric bismuth titanate. Although the device was stable and functional, it required a very large switching voltage, thus making it incompatible with silicon ICs. In addition, it was slow (switching time of the order of microseconds). The slow speed was attributed by Sugibuchi et al[2] to tunnel-injection effects, i.e. charge injected from the silicon surface into traps in the ferroelectric film through the thin native SiO_2 barrier. This resulted in injection type, on/off switching (similar to SONOS) dominating over the desired polarization type switching. Devices in which injection was suppressed by incorporating relatively thick intermediate (buffer) layers of SiO_2 were

demonstrated in subsequent years, using both bismuth titanate[2] and polyvinylidene fluoride (PVF_2)[3] as the ferroelectric gate dielectric. These early FEMFET structures exhibited excessive fatigue, low retention, and degraded programming speed, and required high programming voltages. The FEMFET concept is still recognized as being more desirable than the competing capacitor-type destructive readout for a variety of applications of ferroelectric random access memories because of its nondestructive readout (NDRO) feature. However, there were no further reported attempts to fabricate FEMFETs until the current DARPA sponsored project at Westinghouse. The project was awarded on the basis of a newly developed, proprietary, non-oxide ferroelectric thin film material, BMF, that had the potential for application as the gate dielectric in a FEMFET that was to be designed and fabricated at Westinghouse using standard silicon CMOS processing technology. An alternate (backup) approach was to use a thin film of bismuth titanate as the gate dielectric, with an appropriate buffer layer to prevent the tunneling-trapping type of behavior observed earlier. The $Bi_4Ti_3O_{12}$ films were to be grown by the pulsed laser deposition technique, which provides a much better control of stoichiometry compared to sputter deposition used in earlier Westinghouse work. The early thin film development work, both in BMF and $Bi_4Ti_3O_{12}$, was performed with Westinghouse IR&D funding prior to the start of this contract.

This Interim Report covers the effort on the program through development and testing of FEMFETs fabricated with BMF as the gate dielectric. Also the FERRAM test vehicle is described along with the FEMFET baseline process used to fabricate the wafers.

3.0 TECHNICAL EFFORT

A detailed description of the barium magnesium fluoride (BMF) FEMFET fabrication development and testing is provided in this section. The FERRAM test vehicle is described and the resultant baseline FEMFET fabrication process is presented. The BMF FEMFET electrical test results are provided.

3.1 Barium Magnesium Fluoride (BMF = $BaMgF_4$) Background

3.1.1 Crystal Structure

The isostructural group of fluorides $BaMF_4$, where M is either a divalent 3d transition metal ion (Mn, Fe, Co, or Ni) or a nonmagnetic divalent ion (Mg, or Zn), are known to be piezoelectric materials[4], and in all cases except the Mn and Fe compounds, they also display reversible polarization consistent with ferroelectricity[5]. These orthorhombic materials possess a point-group symmetry of 2mm and have been studied extensively in single crystal form. Keve et al[6] determined the crystal structure of $BaMnF_4$ and showed that the polarization lies along the a-axis parallel to puckered sheets of MnF_6 octahedra. It is postulated that, in the ferroelectric members of this group, polarization reversal involves a tilt of the MF_6 octahedra, which is associated with displacement of the Ba atoms parallel to the [100] axis, as illustrated in Figure 3-1. Saturation polarization values[5] for these compounds range typically from 6.7 to 9.7 $\mu C/cm^2$, while room temperature permittivity values range from approximately 7 to 22. Coercive fields for single crystals were reportedly high (> 50 kV/cm), and available P_s data prior to this work had been obtained only via pulse-switching studies. Physical properties of the $BaMF_4$ family are listed in Table 3-1. Since none of these compounds was available commercially, it was decided to synthesize one of them from the

constituent fluorides by molecular beam epitaxy (MBE) for characterization and evaluation as a candidate for the FEMFET application. An analysis of the relevant physical properties of BaF_2 and MF_2 (M = Mg, Zn, Co, or Ni), listed in Table 3-2, shows that BMF is the most suitable candidate for these studies. BaF_2 and MgF_2 have similar melting and evaporation temperatures, and their vapor pressures were also found to be comparable in the temperature range of interest (1000°C to 1200°C). Thus, it should be possible to deposit BMF thin films by evaporating an equimolecular mixture of BaF_2 and MgF_2 from a single source crucible. As can be seen from Table 3-2, MgF_2 is also the least water soluble of the MF_2 family. However, BMF is expected to have a finite water solubility, and will require a capping layer for protection during CMOS "wet processing" steps. Physical properties of BMF are listed in Table 3-3.

TABLE 3-1: Dielectric Properties of $BaMF_4$ Bulk Crystals

$BaMF_4$	Curie-Weiss Temperature	Melting Point	Room Temperature Spontaneous Polarization	Curie Constant	Strain-Free Dielectric Constant			
					$T^{rm} = 22°C$			T^{mp}
M	T_O(°C)	T^{mp}(°C)	$P_S(\mu C/cm^2)$	C(°C)	ϵ_a^{rm}	ϵ_b^{rm}	ϵ_c^{rm}	ϵ_a^{mp}
Mg	990±5	865±5	7.7±0.3	$2.6x10^3$	8	14	8	21
Zn	810±5	745±5	9.7±0.3	$3.36x10^3$	11	17	10	64
Mn	840±5	755±5	?	$4.17x10^3$	11	15	7	51
Fe	820±5	720±5	?	2.05 ± 10^4	11	17	8	200
Co	880±5	855±5	8.0±0.3	$1.12x10^4$	10	22	8	400
Ni	1320±5	965±5	6.7±0.3	$7x10^3$	8	14	7	20

Ref: M. DiDomenico, Jr., M. Eibschutz, H.J. Guggerhein, and T. Camlibel, Solid State Commun. 7, 1119 (1969).

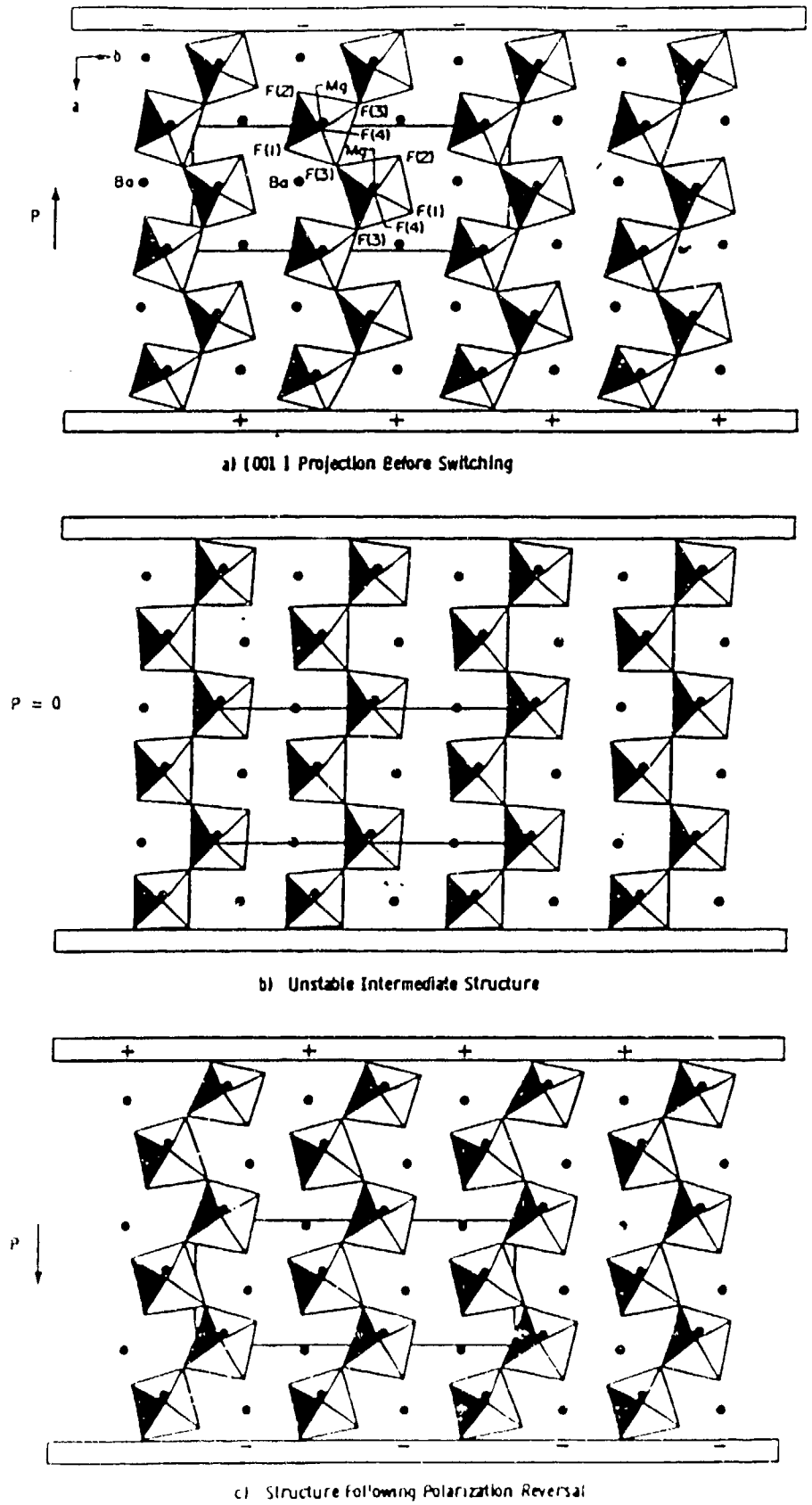
TABLE 3-2: Properties of Selected Difluoride Materials

Material	Density (gms/cc)	Melting Point (°C)	Evaporation Temp (°C) (from vendor catalog)	Water Solubility (gm/100 ml. at 20°C)
BaF_2	4.828	1280	700 (CERAC) 1300-1500 (EM & AC)	0.12
MgF_2	3.148	1266	950 (CERAC) 1300-1600 (EM) 1120-1280 (AC)	$7.6x10^{-3}$
ZnF_2	4.95	872		1.62
CoF_2 $CoF_2.4H_2O$	4.46 2.192	~1200	Decomposes at 200°C	1.5 Soluble
NiF_2 NiF_2-$4H_2O$	4.63	>1000	Sublimes at 1000°C	Slightly soluable

where the vendors are: CERAC, Inc. of Milwaukee, Wisconsin; AC = Atomergic Chemetals Corp of Farmingdale, N.Y.; EM = EM Chemicals of Hawthorne, N.Y.

TABLE 3-3: Physical Properties of BMF

Structure (Symmetry)	Orthorhombic (2mm)
Melting Point	865 ± 5°C
Curie-Weiss Temperature	990 ± 5°C
Spontaneous Polarization (20°C)	7.7 ± 0.3 $\mu C/cm^2$
Lattice Constants	a_1= 5.81.Å a_2 = 14.51Å. a_3 = 4.13Å
Thermal Expansion	
Coefficients (10^{-6}/°C)	α_1 = 11.5. α_2 = 21. α_3 = 20
Dielectric Constants along Polarization Axis [100] at 10 MHz	ϵ_1 = 8.40. ϵ_2 = 14.76. ϵ_3 = 8.24



a) (001) Projection Before Switching

b) Unstable Intermediate Structure

c) Structure following Polarization Reversal

Figure 3- 1: Polarization Reversal in BMF Involves Tilt of the MF_6 Octahedra

3.1.2 Stability of the BMF - Si Interface

Because of the importance of a clean interface between the ferroelectric and the silicon substrate in the FEMFET, the possibility of reactions at the interface was investigated. One possible reaction at the buried interface can be expressed as,

$$BaMgF_4 + Si = SiF_4 + Mg + Ba$$

Since no thermodynamic data exists for $BaMgF_4$, we assume the reaction is

$$BaF_2(s) + MgF_2(s) + Si(s) = SiF_4(g) + Mg(s) + Ba(s)$$

The free energy (ΔG) and enthalpy (ΔH) for the reaction are derived from the free energy (ΔG_f) and heat of formation (ΔH_f) of the fluorides as,

$$\Delta H = \Delta H_f(SiF_4) - \Delta H_f(BaF_2) - \Delta H_f(MgF_2)$$

Using the values of ΔG_f and ΔH_f of SiF_4, BaF_2, and MgF_2 from published thermochemical tables, we derive the values of ΔH to be +171 (at 25°C) and +169 (at 500°C), with the corresponding ΔG values given by +153 (at 25°C) and +134 (at 500°C). For a reaction to proceed, the free energy (and enthalpy) must be at least a negative value. The large positive values of ΔH and ΔG both at 25°C and 500°C indicate that the reactants are thermodynamically stable with respect to the formation of the products, and there is no driving force for the above reaction.

3.2 Thin Film Experimental Methods

3.2.1 Ultra-High Vacuum (UHV) Deposition

Initial BMF film growth experiments were performed (with Westinghouse IR&D funding) in a bakeable ultrahigh vacuum (UHV) chamber equipped with a fluoride sublimation source, an ion gun for substrate surface cleaning, an Auger analyzer for the compositional characterization of the substrate and the film, and a low energy electron diffraction (LEED) unit for the determination of the crystallinity of both the substrate and the film. This experimental setup had been used previously[9,10] for the growth of epitaxial group II fluorides on semiconductors. The base pressure in the baked UHV chamber was less than 1.0×10^{-10} Torr. The substrates were cut in the form of 0.75 inch square pieces from wafers and mounted on the molecular beam epitaxy (MBE) type sample holder. Bulk single crystal pieces of BMF, Czochraski grown in an isolated growth chamber using optical grade BaF_2 and MgF_2 as starting materials were obtained from Sanders Associates, Inc, Nashua, N. H. (courtesy of T. M. Pollak), and were used as the source in the evaporator. BMF films were also grown successfully by evaporating BaF_2 (99.995% pure) and MgF_2 (99.99% pure) powders (Johnson Mathey) mixed in equimolecular proportions and ball-milled prior to insertion in the UHV chamber.

Following the initial verification of stoichiometry, crystallinity, and ferroelectricity in the BMF thin films, film growth was shifted to a commercial V80H MBE system from VG Instruments, Inc., shown in Figure 3-2. The V80H MBE system, originally designed for 3-inch wafers, was modified (IR&D funded) to accommodate 4-inch diameter silicon wafers. The modification process, which involved changes in the design of the substrate holder in the growth chamber, the transfer mechanism, and the cassette holder in the entry chamber, has been described in detail in a Journal of Vacuum Science and Technology Shop Note.[11] The changeover from the small chamber to the VG V80H system, and the modification from 3-in. to 4-in. wafer capability was required for wafer size compatibility with the existing standard VLSIC processing during device fabrication before and after ferroelectric film growth.

Three different types of 4-inch diameter silicon wafers were used as substrates. Initially, high conductivity (0.005 - 0.02 Ω-cm) n-type wafers were used to facilitate measurement of hysteresis and dielectric properties of the BMF films. C-V measurements were performed on films grown on p^-/p^{++} (3μm p^- epitaxial Si layer on a p^{++} wafer) or gridded (n^+ grids in p^- epitaxial Si layer on a p++ wafer) wafers. Silicon substrate cleaning prior to insertion in the MBE chamber consisted of the several steps listed in Table 3-4. Step 4 in the cleaning procedure provided a fluorine passivation layer which could be removed by thermal anneal inside the MBE chamber. The procedure was simplified by skipping step 3, after electrical characterization of the BMF showed that step 3 could be eliminated without adversely affecting the capacitance-voltage (C-V) characteristics of the films. In those cases where film growth was desired on a SiO_2 coated surface, only steps 2 and 4 were used. For film growth on patterned, semi-processed silicon wafers, the procedure had to be modified further. In these cases, in addition to eliminating step 3 and the first part of step 4 (1:5 $HF:H_2O$), the trichloroethylene in step 2 was replaced by acetone. In-situ thermal cleaning consisted of anneals at temperatures ranging from 500°C to 900°C, depending on the substrate. However, after some initial experimentation, anneal at 520°C for 20 minutes was the standard procedure. The BaF_2 + MgF_2 mixed powder was evaporated from a pyrolytic graphite crucible. Boron nitride crucibles were not used because of the possibility of boron contamination in the BMF films. The crucible temperature during film growth was maintained at 1075°C to 1100°C, resulting in a growth rate of about 0.2 nm/sec. Films were grown at substrate temperatures ranging from 200°C to 600°C. Film thicknesses ranged from 100 nm to 500 nm.

3.2.2 Post-Deposition Thermal Annealing

During the course of these studies it was found that BMF film structure was very sensitive to both deposition temperature and subsequent annealing conditions. In both cases, modification of temperature and/or gaseous ambient could lead to significant changes in crystallinity and crystallographic orientation. These effects are described in subsequent sections of this report. Initially, post-deposition thermal annealing was employed in-situ (in the UHV system, immediately after MBE growth) in order to crystallize the amorphous BMF film deposited at the low growth temperature. Subsequently, annealing was carried out "ex-situ" in a separate furnace system, usually in flowing hydrogen or forming gas (90% nitrogen + 10% hydrogen). Furnace-annealing involved rapid insertion of the film sample into the hot zone of the furnace, followed by isothermal treatment for periods from 30 to 60 minutes. Later, rapid thermal annealing (RTA) in forming gas (using a commercial A. G. Associates Model 410 system) was employed in order to achieve better control of crystal orientation and electrical properties.

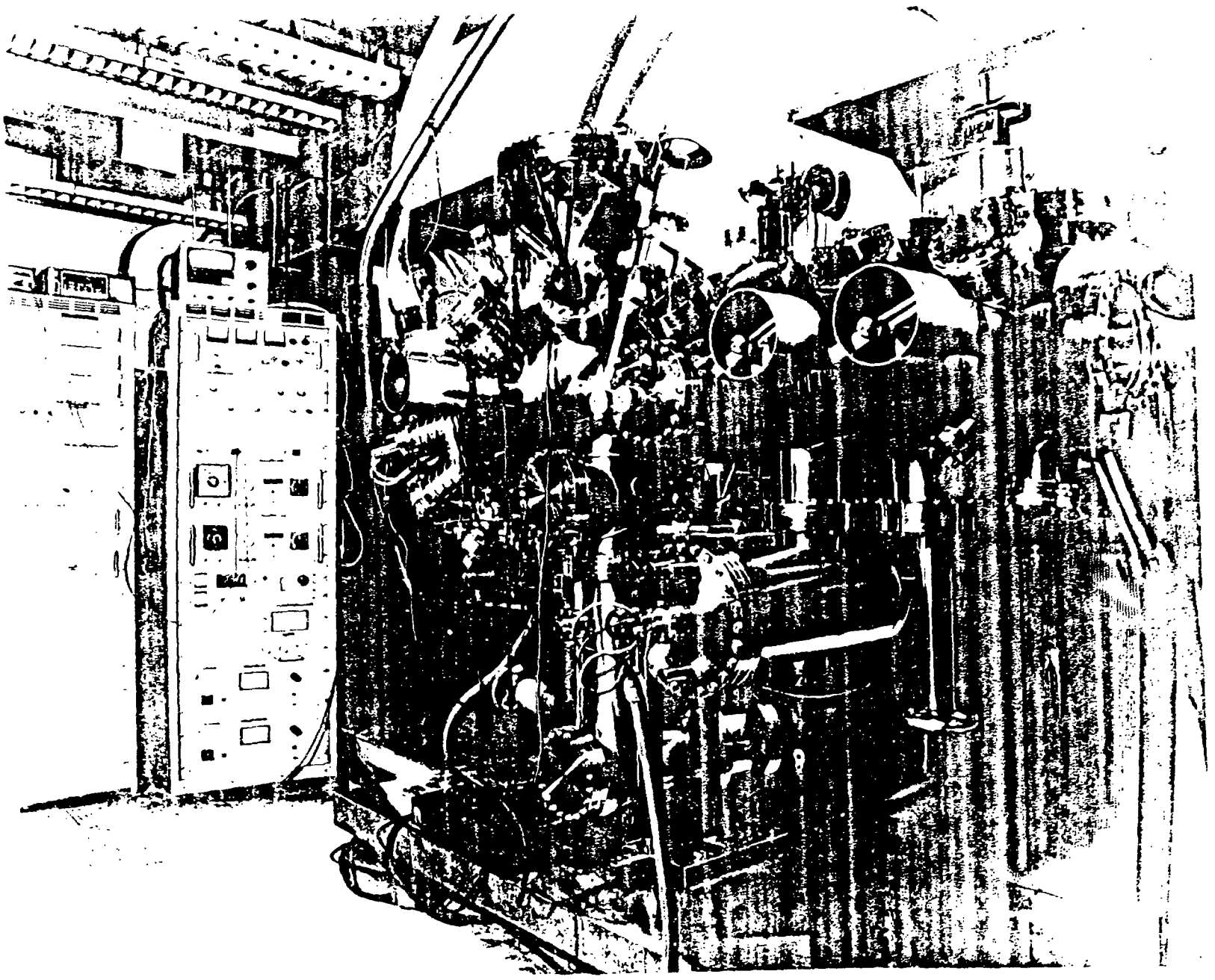


Figure 3-2: The V80H MBE System

TABLE 3-4: Silicon Substrate Cleaning Steps

Step 1: Buffered HF (NH_4F+HF) (6:1) etch for 15 to 30 Seconds to remove oxide, followed by deionized water rinse (10 Minutes).

Step 2: Degrease:

- Ultrasonic cleaning in mehtanol for 10 Minutes
- 15 Minuted in boiling trichloroethylene
- Ultrasonic cleaning in methanol for 10 more Minutes
- 10 Minutes in flowing deionized water

Step 3: RCA Procedure (to be repeated once):

- 15 Minutes in ($H_20+NH_4OH+H_20_2$) (5:1:1) at 80°C, followed by 5 Minutes deionized water rinse
- 15 Minutes in ($H_20+HC1+H_20_2$) (5:1:1) at 80°C, followed by 5 Minutes. DI-water rinse first time and 10 Minutes. the second time

Step 4: Fluorination:

- $HF+H_20$ (1:5) dip for 45 Seconds
- $HF+H_20$ (1:50) dip for 45 Seconds, spin dry

3.2.3 Structure and Composition Characterization

The vacuum-deposited BMF film samples were characterized structurally by a number of X-ray diffraction methods (and in a few cases by electron microscopy) depending on the crystalline condition of the deposit. X-ray powder photography (Debye-Scherrer) and diffractometry (including double-crystal techniques) were used primarily for phase identification and for studies of preferred orientation. These were supplemented in some cases by texture camera evaluation. Oscillation and Weissenberg single-crystal techniques also were employed on selected film samples in order to determine epitaxial relationships for films grown at higher substrate temperatures. In some cases transmission (TEM) and scanning (SEM) electron microscopy were used to study crystal size and orientation and to evaluate structural continuity of the films. The phase composition (and assumed chemical composition) could be estimated to a sensitivity of about 2% for well-crystallized film samples. For this analysis X-ray pattern reference data obtained from pure single-crystal samples of BMF were employed.

3.2.4 Dielectric Electrical Measurements

A mercury probe was used extensively for the dielectric and ferroelectric characterization experiments on the BMF films. Shadow-mask-evaporated Al dot patterns and a standard probe station were also used in the case of SiO_2-capped BMF films. Metal (Al, Cr-Au) dot patterns could not be used successfully on uncapped films because of leakage problems. Attempts to grow BMF films on platinum or nickel coated silicon were

not successful due to apparent reaction between the metal and the film. A modified Sawyer-Tower bridge and a RT-66A test system (Radiant Technologies Inc., Albuquerque, NM) were used for the ferroelectric characterization of the films. Capacitance and conductance measurements were performed first with a Boonton model 75C direct capacitance bridge, and later with a Hewlett Packard 4284A LCR meter (20 Hz to 1 MHz).

3.3 Deposition Experiments and Results

Some of the key parameters for successful operation of thin-film ferroelectric memories (whether of the capacitor or integrated FEMFET type) are low-voltage address (approximately 5V or less), low threshold field (E_c) for ferroelectric switching, large value of switched polarization (P_s), low permittivity (ϵ), high breakdown field and low dielectric leakage - associated with high charge-storage stability (retention) and low ageing and fatigue. The inter-relation between polarization, coercive field and permittivity has been expressed by Scott et al.[12] as an operating figure of merit $P_s/((\epsilon)(E_c))$. Address voltage can be reduced (for a given threshold, or coercive field) simply by reducing the ferroelectric film thickness. However, for typical polycrystalline film structures, lowering the thickness much below 100 nm is impractical, since discontinuities, pinholes, and cracks become more numerous and result in premature dielectric breakdown. Improved structural continuity can be achieved by using lower processing temperatures, but this can lead to degraded stoichiometry and crystallite quality, which in turn raises the intrinsic coercive field. It has been pointed out by Smyth[13] that the ferroelectric switching fields used for typical film structures already approach the dielectric breakdown strength, and that this can lead to field-induced migration of ions and defects with deleterious effects on memory stability.

The above comments are applicable to any ferroelectric film material suitable for use in capacitor- or FEMFET-type device structures. However, special additional considerations arise in the case of BMF ferroelectric films. Unlike pseudo-cubic oxide perovskite materials (e.g. PZT) which display multi-axial polarization switching behavior due to their higher crystal symmetry, BMF has uniaxial polarization characteristics, with P_s lying parallel to the orthorhombic a-axis. It is clear that for such a structure the highest P_s/E_c ratio would be obtained for an epitaxial film in which the polar axis lies perpendicular to the substrate. It is also evident (as we discuss later) that for a randomly oriented BMF film structure (unlike the case of a randomly oriented PZT film) some regions of the film will require switching fields far exceeding those causing dielectric breakdown. Data reported here for thinned bulk crystal samples of BMF suggested at the outset of these studies that switching fields required for thin films would be high. However, the low permittivity of BMF partly counterbalances the high E_c, to give an attractive figure of merit value in Scott's expression quoted above.

A strong positive attribute of BMF for use in FEMFET device structures is its chemical compatibility with silicon. Our studies prior to the beginning of this contract convincingly demonstrated that UHV deposition of BMF on clean silicon surfaces resulted in very low interface state densities. It was also found that relatively wide memory voltage windows (approximately 10V) could be obtained in MIS structures with modest values of switched polarization (approximately 0.2 $\mu C/cm^2$). Based upon preliminary studies conducted at Westinghouse before the award of this contract, it was believed that transistor structures exhibiting high performance FERRAM-FEMFET operation could be achieved by incorporating UHV-deposited ferroelectric BMF films, in the thickness range 100-200 nm, as the gate dielectric on (001) Si

substrates. In accord with the above comments, our goal has been to vary systematically deposition and annealing conditions, and through correlative analysis and electrical studies to establish fabrication procedures suitable for construction of high-performance and stable FEMFET memory cells and arrays. The following sections outline in detail the research steps, analytical and measurement data, and iterative procedures involved.

3.3.1 Structure Versus Deposition and Annealing Conditions

Initially, BMF films were grown at relatively high temperatures (400 to 600°C) in the hope of obtaining epitaxial films with the polarization axis perpendicular to the surface. Structural and compositional analysis indicated that UHV deposited films possessed essentially the desired BMF stoichiometric composition at all growth temperatures lower than 650°C. Growth at temperatures above 400°C yielded mixtures of (010) fiber-oriented and randomly oriented components. In the usual case of growth on clean (001)Si at higher temperature, these components were accompanied (or supplanted) by epitaxial components. At temperatures of 500°C or higher, multiple epitaxial structures were developed; these are illustrated in Figure 3-3. For each epitaxial component the orthorhombic (011) plane of BMF lies parallel to the (001)Si substrate plane. The components can be generated from each other simply by a rotation of 90° about the normal to the BMF(011) plane. The occurrence of the (010) fiber texture at lower temperature is consistent with the strong tendency for BMF single crystals to cleave on this plane. Polarization hysteresis measurements of these films using a mercury probe showed a very narrow hysteresis loop, with little remanent polarization. This is consistent with the fact that the ferroelectric a-axis of these films lies parallel to the substrate surface, with no component of polarization aligned to the applied field. For use of BMF films as a gate dielectric in FEMFET memory structures, it is essential that at least a component of the polarization should lie normal to the substrate. In the growth structures described above, this does not occur in the higher temperature epitaxial deposits. No epitaxial conditions were able to be established for which the ferroelectric a-axis lies perpendicular to the film plane. Thus, to obtain significant ferroelectric switching it appeared necessary to utilize samples which are randomly oriented, or display only weak (010) fiber textures. Since the (010) fiber orientation seems to be a growth texture, we believed that a more random orientation might be favored by resorting to thermal annealing of amorphous deposits. During the course of these studies several annealing conditions were examined, including in-situ vacuum annealing, vacuum furnace annealing, furnace annealing in hydrogen or forming gas, and rapid thermal annealing (RTA) in forming gas. The two latter methods were emphasized, since they were more compatible with semiconductor integrated circuit (IC) processing.

Table 3-5 shows representative data from the annealing studies. The key trends for films which were vacuum furnace-annealed for periods of 30 to 60 minutes can be summarized as follows. Annealing at 600°C of films grown at 350°C (the highest temperature at which an amorphous growth structure was observed) produced a weak (010) fiber texture, associated with a minor randomly oriented phase. This random phase could be accentuated markedly (essentially eliminating the fibered component) by annealing films which were grown at lower temperatures, preferably in the range of 150°C to 250°C. Thus, for films grown at 200°C, annealing in hydrogen at 480°C reproducibly resulted in an almost perfectly random orientation. (The electrical characteristics of both of these samples and of (010) fiber-oriented BMF films are described in the following section.) The orientation changes with annealing are effectively illustrated in the X-ray diffractometer traces in Figure 3-4. The use of higher growth temperatures invariably produced, after annealing, a more fiber-oriented structure. This appeared to indicate that at growth

temperatures in the range of 250°C to 350°C microcrystals with the (010) fiber orientation had already nucleated in the deposited film. The use of lower annealing temperatures also favored a more fibered structure. When the annealing temperature was raised slightly above 500°C, part of the randomly oriented film structure was supplanted by a (011) epitaxial component. Annealing in hydrogen at temperatures above 550°C generally resulted in partial decomposition. This was recognized through the appearance of a (001) oriented BaF_2 phase, evidently caused by selective loss of MgF_2.

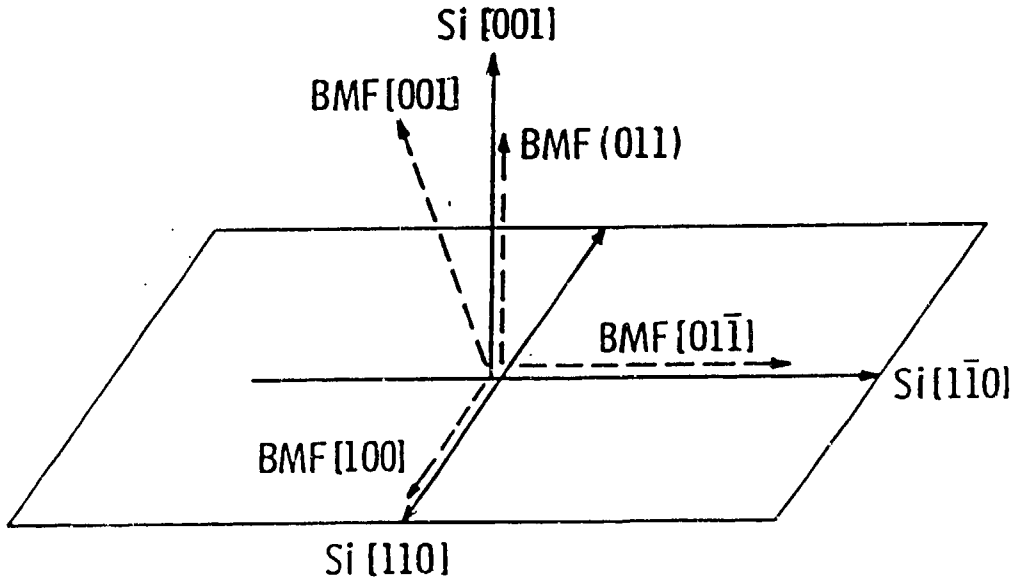
Somewhat different results were obtained for films which were RTA-processed in forming gas for much shorter time periods (5-10 seconds). The preliminary data from this study are shown in Table 3-5. Essentially, all films annealed under RTA conditions in the temperature range 550°C to 700°C displayed completely random orientation of a single ferroelectric BMF phase, with no evidence of decomposition at the higher end of the temperature range. We attribute this in part to the shorter annealing time, and also to the far lower content of hydrogen (10% in nitrogen) in the annealing atmosphere. The RTA results have an important bearing on the hysteresis properties of the films and on the memory retention and stability behavior.

The composition of the BMF-Si interface was analyzed using Auger Electron Spectroscopy (AES). Auger depth profile of a 170 nm thick BMF film grown at 350°C and subsequently vacuum-annealed at 500°C for 60 minutes is shown in Figure 3-5, where Auger signal heights of the relevant elements have been plotted as a function of depth into the film and then to the silicon substrate through the interface. The results show that trace amounts of carbon (C) and oxygen (O) are still present at the interface. However, their presence does not appear to affect the electrical properties of the interface, as described in the next section. The non-zero silicon Auger signal inside the BMF film is an artifact caused by interference effects in the Auger window chosen for the depth profile, and should be discounted.

EPITAXIAL ORIENTATIONS

Ba Mg F_4 Film

(BMS-3)



- One of the four components shown
- Generate others by rotating 90° about BMF (011) three times

Figure 3- 3: Multi-epitaxial Orientations of BMF Films

TABLE 3-5: Representative data from BMF annealing studies using 150-300 nm films.

Growth Temp. (°C)	Post-anneal Conditions	Film Structure (X-ray)
150 - 375	None	Amorphous or microcrystalline
350	Vac-anneal 1 hr each at 400, 500, 600, 700°C	(011) multiple epi structure + (010) fiber tex. each case.
350	Vac-anneal 600°C, for 30 minutes	Multi-epi + more (010) fiber, or poly + multi-epi as above.
300	H_2-anneal 1 hr each at 400°C 500°C 600°C 700°C	 Amorphous * Poly + some (011) orientation Poly + fiber-texture BaF_2 Only (100) fiber-texure BaF_2
200	H_2-anneal 1 hr each at 480°C 500°C 550°C	 Polycrystalline Poly + some (010) fiber-tex. Preferred (010) + some poly.
200	Forming gas (N_2 + 10% H_2) anneal at 480°C, 1 hr.	Preferred (010) fiber texture with some poly component.
150	Vac-anneal, 480°C, 1 hr H_2-anneal, 480°C, 1 hr	Poly + some preferred (010) Poly + some preferred (010)
150	RTA in forming gas: 550°C for 10 seconds 600°C for 10 seconds 650°C for 5 seconds 700°C for 5 seconds	 Polycrystalline film Polycrystalline film Polycrystalline film Polycrystalline film

* Unless otherwise indicated, phases described as "poly" or polycrystalline are randomly oriented.

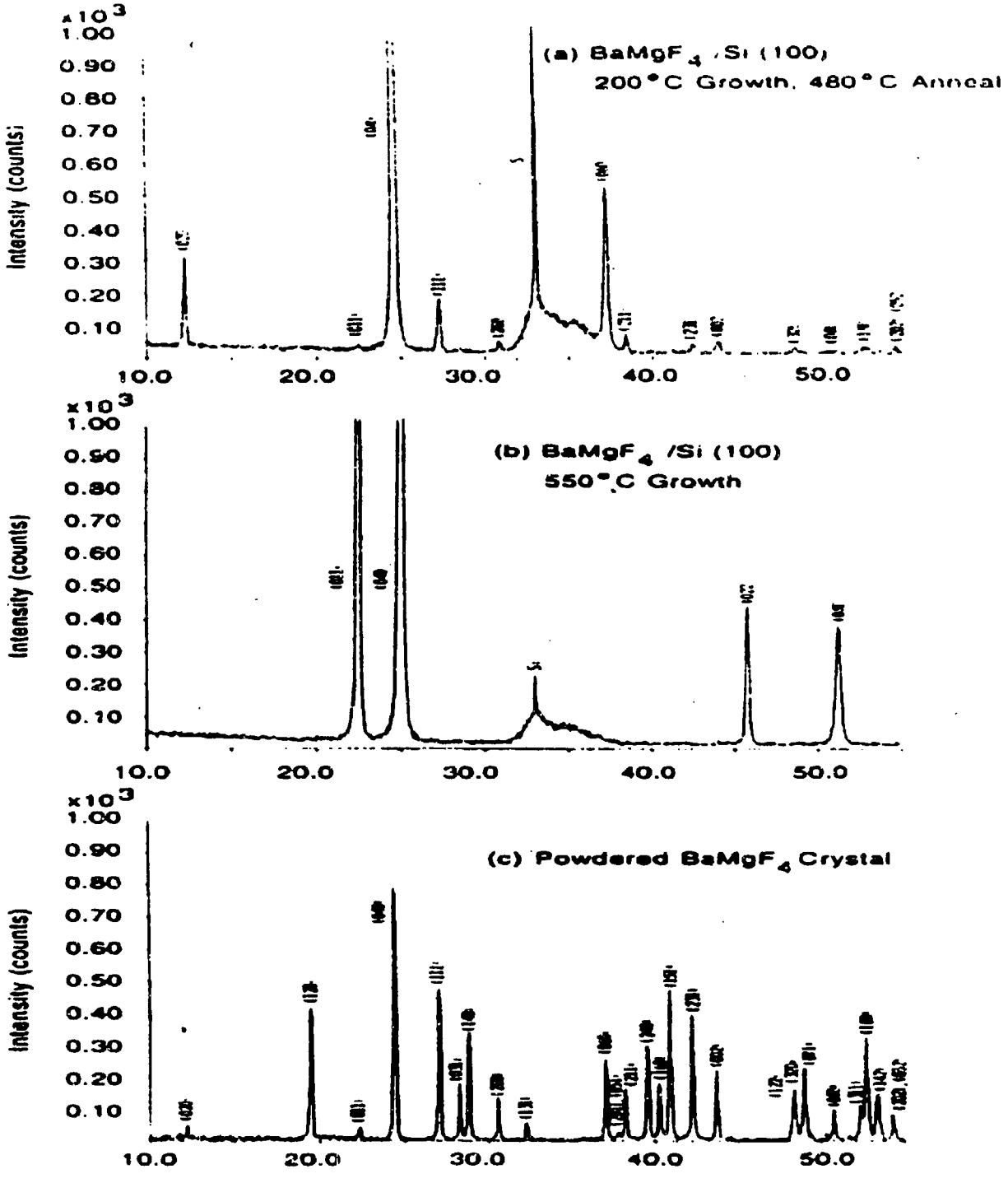


Figure 3- 4: X-ray Diffraction Results for BMF Films Prepared Using Different Deposition and Post-Anneal Conditions.

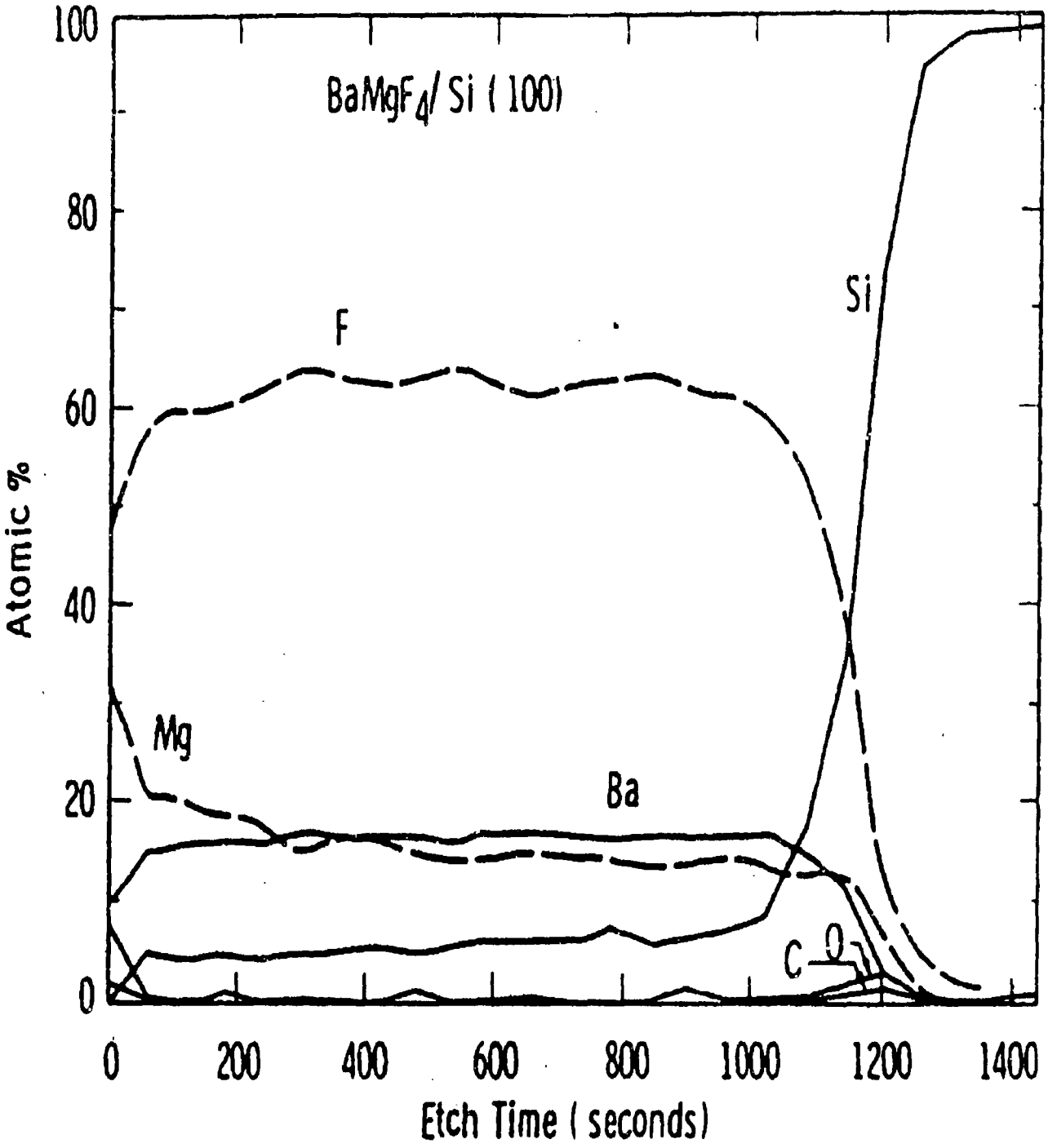


Figure 3- 5: Composition of the BMF-Si Interface (Initial BMF Film Thickness ≈ 250 nm.)

3.3.2 BMF Film Stress Versus Temperature

Two four inch silicon wafers (P-/P++) were prepared with BMF thin films deposited at 200°C to a thickness of 360nm on one and 180nm on the other. These wafers were then sent to Professor Seshu Desu at the Virginia Polytechnic Institute (VPI), Department of Material Engineering, where they were evaluated for stress in the BMF films. The 360nm film showed an initial tensile stress around 220MPa. Upon heating in argon atmosphere, the stress decreased (in the direction of compression) which indicated that the thermal expansion coefficient of BMF is larger than that of the silicon substrate. There was a break of linearity around 250°C and the stress leveled at around 50 MPa and remained constant on annealing for one hour at 500°C. Then the stress increased linearly during cooling down to 80°C. The final stress after annealing was around 500 MPa. Figure 3-6 shows the stress versus temperature for the 360nm thick film. The second sample with the 180nm BMF film showed an initial tensile stress around 170 MPa and the final stress after annealing in hydrogen was around 420 MPa in tension. The stress-temperature plot was similar to the one obtained on the 360nm film. The major difference was that overall stress values were lower.

After measurement, both samples were returned to Westinghouse where they were capped with 500Å low temperature oxide (LTO) at 400°C. Then both samples were sent back to VPI for stress measurements to determine how the LTO caps affected the stress. After capping the 360nm film showed a tensile stress of around 207 MPa. The final tensile stress, after annealing in hydrogen at VPI, was around 320 MPa. Figure 3-7, the stress-temperature plot, shows linear slopes which indicated that no noticeable transformation occurred during heating and cooling. Increased tensile stress was observed when the sample was held at 500°C for one hour indicating continued crystallization of the BMF.

3.4: Electrical Measurements

3.4.1 Thin "Bulk" Single Crystal

A thinned single-crystal sample of BMF (cut perpendicular to the a-axis) was characterized electrically to provide reference data for subsequent evaluation of thin films and to verify the ferroelectric polarization results reported earlier by Eibschutz et al[5] who used the pulse switching technique. Thinning of the single crystal piece was achieved by first cutting (with a string saw) a flat piece of the material with the [100] axis perpendicular to the flat surface. The surface on one side was polished with No. 3 and No. 1 diamond and then coated with a 500 nm thick film of Ti-Pt. The sample was then mounted with blanchard epoxy, coated surface down, at the center of a flat ceramic piece that had a 1.6 mm-diameter hole at the center for the purpose of making electrical contact with the Pt-coated surface. The mounted BMF single crystal piece was next polished with No. 3 and No. 1 diamond for thinning. However, cracking parallel to the (010) cleavage plane, and subsequent chipping of the single crystal piece was observed during the polishing, limiting the lowest thickness obtained to 10 μm. Initially Al, and later Cr-Au dot patterns were deposited on this foil for characterization. Contact with the back surface was established by dissolving the epoxy at the bottom of the hole in the ceramic plate with acetone and contacting the Ti-Pt back coating with a thin gold wire and silver paste.

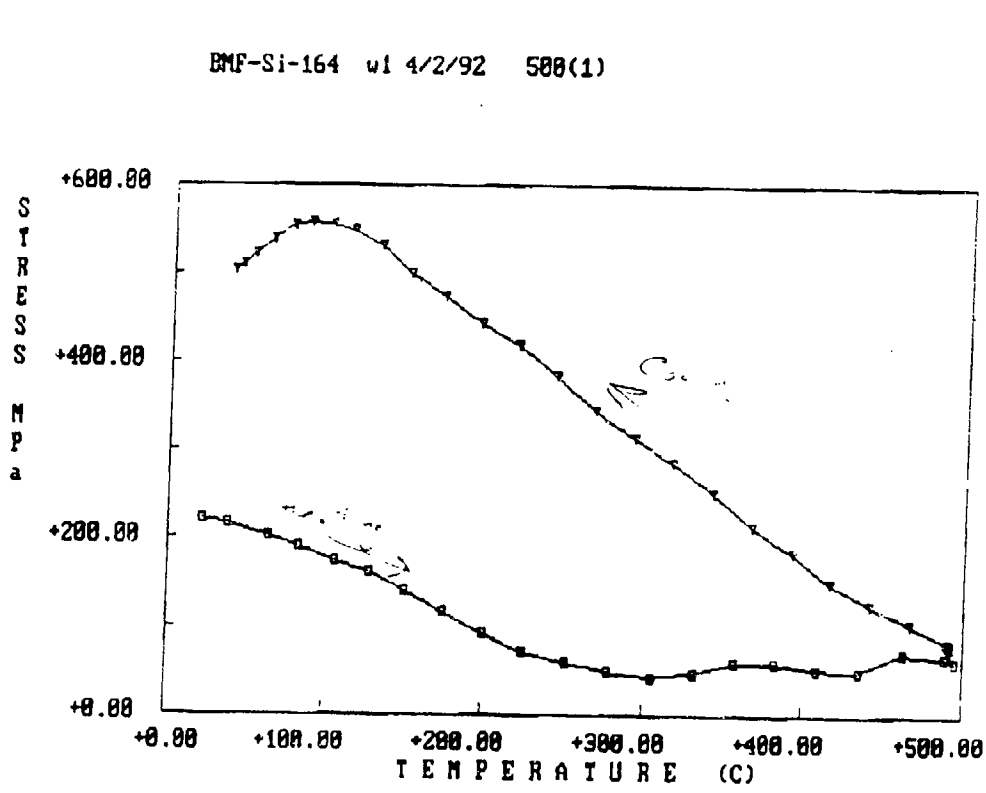


Figure 3- 6: Stress vs Temperature for a 360nm Thick BMF Film on 4-inch Silicon Wafer (Measured by Professor Seshu Desu at Virginia Polytechnic Institute)

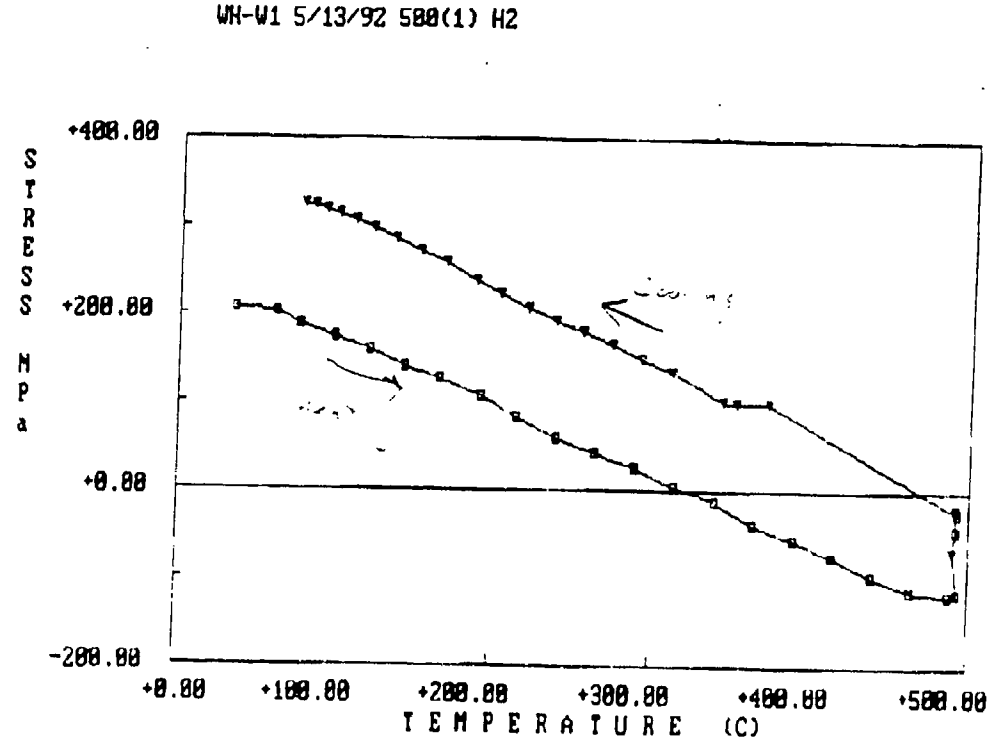


Figure 3- 7: Stress vs Temperature for the Above 360nm Thick BMF Film After Capping With 500Å of Low Temperature SiO_2 (Measured by Professor Seshu Desu at Virginia Polytechnic Institute)

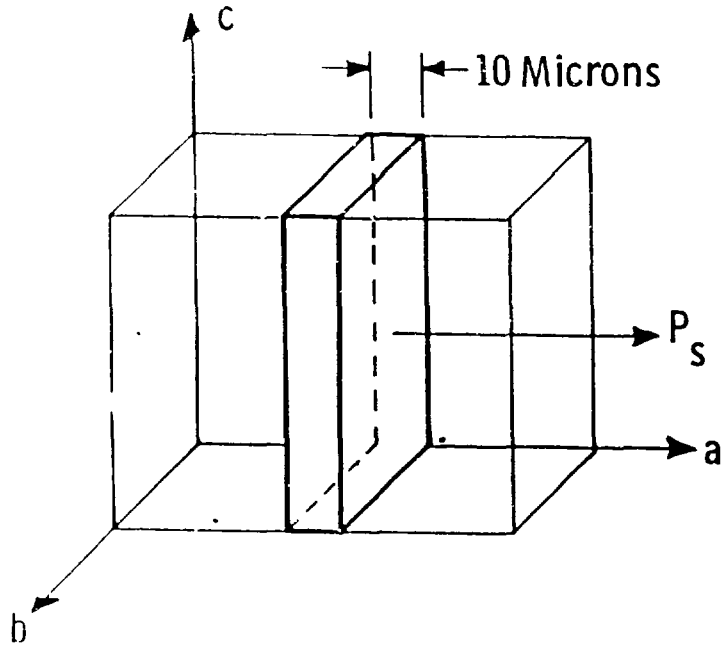
A hysteresis loop obtained at 2 kHz with the thinned, 10 μm thick BMF (100) single crystal is shown in Figure 3-8 together with a sketch of the morphology and orientation of the crystal. The evaporated aluminum top electrode had a diameter of 850 μm in this case. Breakdown occurred at slightly higher voltages, prior to saturation. The loop, although not completely saturated, shows a remarkably high degree of squareness ($P_r/P_s > 97\%$) at an applied voltage of 120 Volts. This result agrees very well with the data published by Eibschutz et al.[5] who measured the spontaneous polarization of $BaMF_4$ family of fluorides by the pulsed-field technique. Their results showed that, typically, more than 99% reversal of the spontaneous polarization was achieved on the application of the pulsed field. The spontaneous polarization (P_S) and the coercive field (E_c) values for the BMF single crystal were calculated from the hysteresis loop, shown in Figure 3-8(b), and were found to be 8.5μC/cm^2 and 95.4 kV/cm, respectively. The P_S value is somewhat higher than the value of 7.7 μC/cm^2 reported by Eibschutz et al.[5] for this material.

3.4.2 Thin Film Data and Analysis

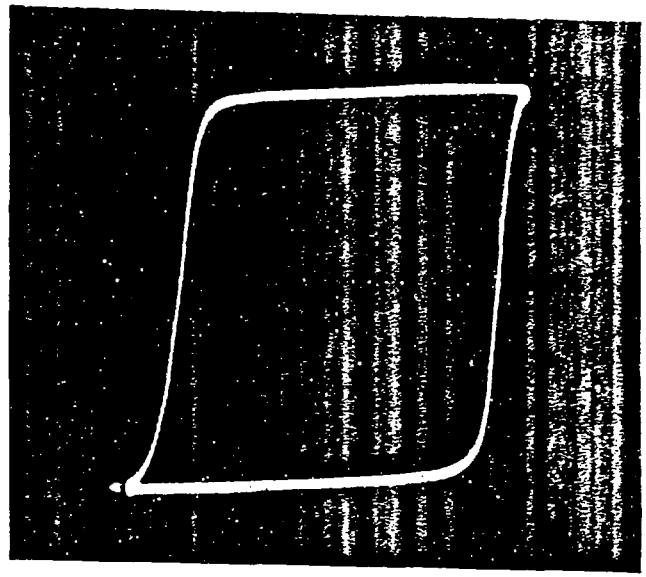
3.4.2.1 Films Without Dielectric Capping Layers

The first thin film samples prepared during this portion of the program were deposited at 350°C and vacuum furnace annealed at 600°C (cf. data in Table 3-5). The weakly oriented (010) texture developed after this treatment is depicted in Figure 3-9, which shows the Debye-Scherrer X-ray pattern of the film (obtained under glancing angle conditions) compared with that of a randomly oriented powder sample. Supplementary X-ray oscillation patterns confirmed the main (010) fiber structure, and also indicated the presence of a weak secondary (011) epitaxial component. Data for the fiber-textured structure suggested that the ferroelectric a-axis lay approximately parallel with the Si substrate surface, with an angular spread of about $\pm 25°$ to $\pm 30°$.

Initial attempts to obtain hysteresis data from 200 nm thick BMF film samples, deposited at 350°C and vacuum annealled at 600°C, often yielded only conductivity loops. However, within a few seconds after application of somewhat higher fields (approximately 500-600 kV/cm), well-developed hysteresis loops began to form, growing in amplitude as the applied field was increased up to the breakdown voltage of approximately 10^6 V/cm. The final loop shape, just prior to breakdown, using a mercury probe test system with an effective contact area of approximately 4.07×10^{-3} cm^2, is illustrated in Figure 3-10. P_S and E_C values calculated from this hysteresis loop were found to be 1.6 μC/cm^2 and 175 kV/cm, respectively. The value of P_S measured for this film sample is significantly lower than that obtained from the single crystal described above (i.e., 1.6 μC/cm^2 compared to 8.5 μC/cm^2). The coercive field of 150 kV/cm for the thin film is rather high, but not inconsistent with the bulk crystal data (E_c = 95.4 kV/cm along the ferroelectric a-axis). In part this high value can be attributed to the field values needed to switch those components of polarization lying nearly parallel to the substrate surface.



(A) Morphology and Orientation of Crystal Sample Cut Perpendicular to a-Axis



(B) Hysteresis Loop at 2 kHz. Scale: Vertical, 3.75 $\mu C/cm^2$ per Large Division; Horizontal, 47.7 KV/cm per Large Division. (E_c = 95.4 KV/cm)

Figure 3- 8: Orientation and Hysteresis Measurement of Thin Bulk Single Crystal BMF Sample

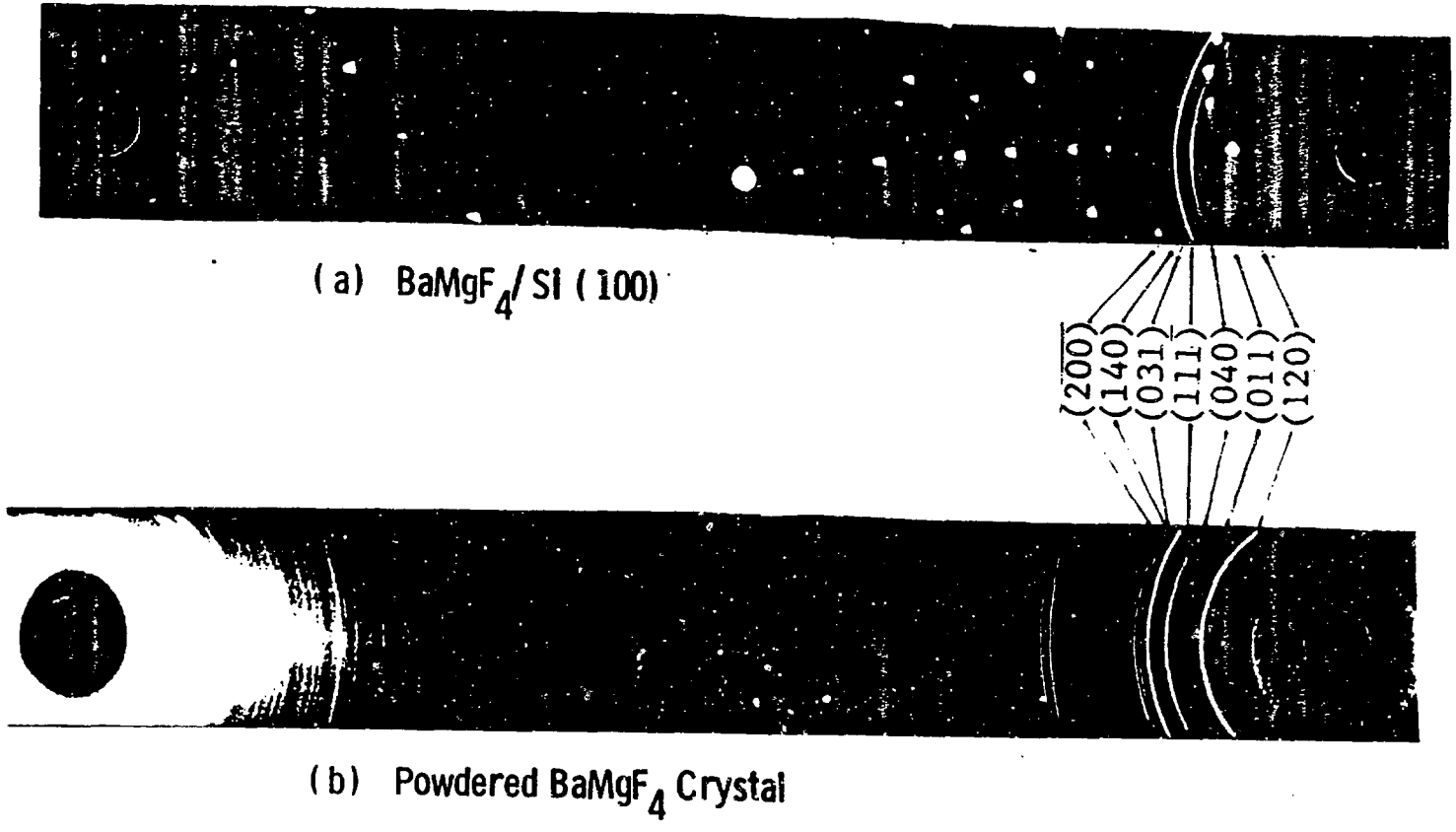


Figure 3- 9: Debye-Scherer X-Ray Patterns Comparing BMF Film and Powder

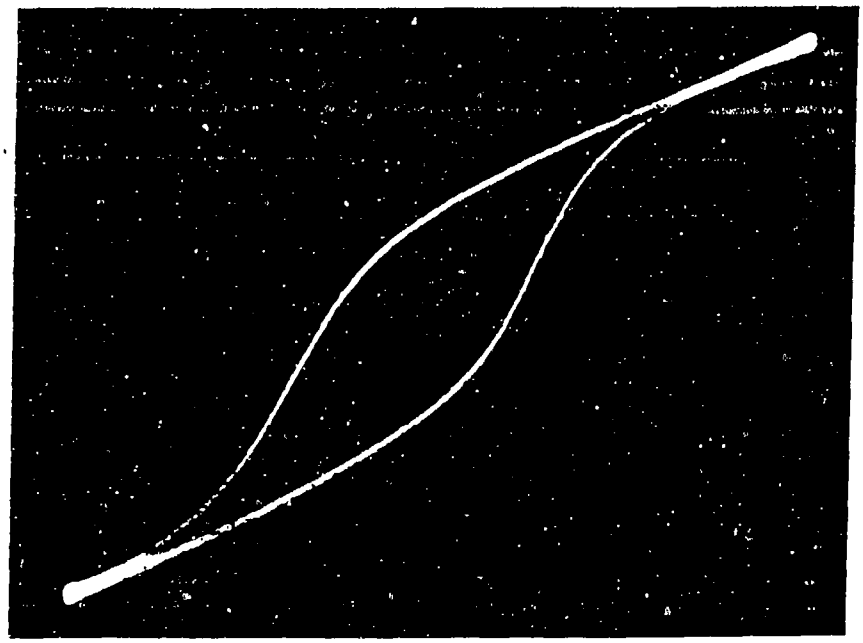


Figure 3-10: Hysteresis loop of a 200 nm thick UHV-grown BMF film on Si(100) The film was grown at 350°C and then vacuum annealed at 600°C. Vertical scale: 1.2μC/cm^2 per large division; horizontal scale: 250kV/cm per large division. (P_s = 1.6 μC/cm^2, E_c = 175 KV/cm)

The switching properties of polycrystalline films of a uniaxial ferroelectric such as BMF lend themselves readily to simple analysis, since in constituent grains we are dealing only with 180° domain boundaries. We can model the switched polarization vs. switching field behavior simply by assuming that for each grain, reversal of P_s occurs when the field component E_s parallel to its a-axis attains a value exceeding that needed to switch a single crystal sample (cf. Figure 3-8), as depicted in the sketch of Figure 3-11. When the threshold switching field is assumed about 95.4 kV/cm. (based upon the results in Figure 3-8) and the polarization axes in a fiber-textured sample are uniformly distributed within the angular range measured by X-ray techniques, a simple integration procedure over that range can be used to plot the calculated value of switched polarization against the actual applied field $E_s/\sin\propto$. Typical plots are shown in Figure 3-12 for the fiber-textured sample measured here and also for a randomly oriented sample. If we further assume that the switching fields required for the fibered film sample are actually a factor of two higher than those derived from bulk single-crystal data, an excellent match is achieved in Figure 3-12 between the calculated and experimental results.

As expected from the structural evaluation described above, much higher values of switched polarization were obtained from more randomly oriented BMF film samples produced by alternate annealing conditions shown in Table 3-5. Figure 3-13 shows, for example, a family of hysteresis loops from a film comprising mainly randomly oriented material with a weak (010) fiber-textured second phase. At an applied field amplitude approaching 1,000 kV/cm, the estimated value of P_s switched was about 3.6 $\mu C/cm^2$. As indicated by comparing Figures 3-10 and 3-13, the squareness ratios for these higher P_s films was also higher, attaining typical values of 93%. For more recent film samples comprising almost entirely randomly oriented BMF crystallites, the value of P_s measured has been as high as 4.55 $\mu C/cm^2$. This is in excellent agreement with the value of 5.25 $\mu C/cm^2$ calculated for a randomly oriented film structure (see upper plot of Figure 3-12). However, most films broke down well before these values of P_s were attained.

Dielectric permittivity and dissipation factor were measured for a fiber-textured film grown on silicon, and are plotted for the frequency range of 5 to 500 kHz in Figure 3-14. The permittivity displays some variation with frequency, falling from a value of 9 at 5 kHz to 8.4 at 500 kHz. This compares rather closely with the average value of 10 reported by DiDomenico et al.[7] for bulk single crystals, which were also found to show dispersive permittivity at lower frequencies. This low value of permittivity, compared with those typical of oxide ferroelectric materials, provides a significant advantage (factor of 10 or better) in relation to the figure of merit expression used by Scott et al.[12]

In the early stages of this program results on thermally annealed films were somewhat erratic, and in many cases premature breakdown was observed, probably by grain-boundary conduction at cracks generated by the high temperatures used in annealing. C-V measurements were successfully attempted on multiple-epitaxial BMF films grown at 550°C on standard 4-inch diameter VHSIC CMOS Si(100) wafers (8-10 μm of 4-8 Ω-cm epi Si on 0.005-0.02 Ω-cm silicon substrate). A typical C-V plot, obtained from a 200 nm thick film, using a mercury probe is illustrated in Figure 3-15. The C-V curve exhibits many features of the expected ideal behavior[14] of ferroelectric films on silicon for use in nondestructive readout (NDRO) nonvolatile memory devices. The most prominent attribute is the 14 Volt threshold shift (generally called the "memory window") in response to the ±20 V programming voltage. The C-V hysteresis loop was scanned at a rate of 75 mV/sec at room temperature, with a clockwise trace indicated by the arrows. The

clockwise direction of the C-V loop is indicative of polarization charge reversal inside the ferroelectric layer, rather than by tunnel injection of carriers from the silicon into the ferroelectric.

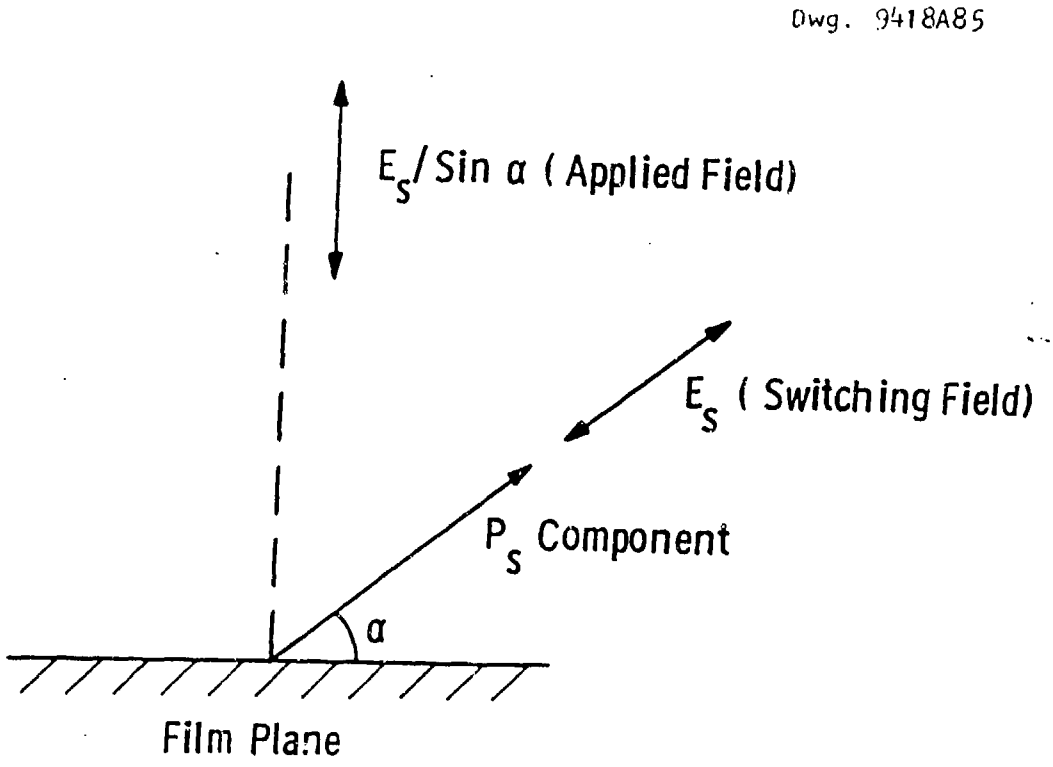


Figure 3-11: Calculation Approach: Using Value of Switching Field (Derived from Bulk or Epi Data), Polarization Component "$\underline{P_S} \cdot \underline{d\alpha}$" Plotted Against Applied Field "$E_S/\text{Sin } \alpha$"

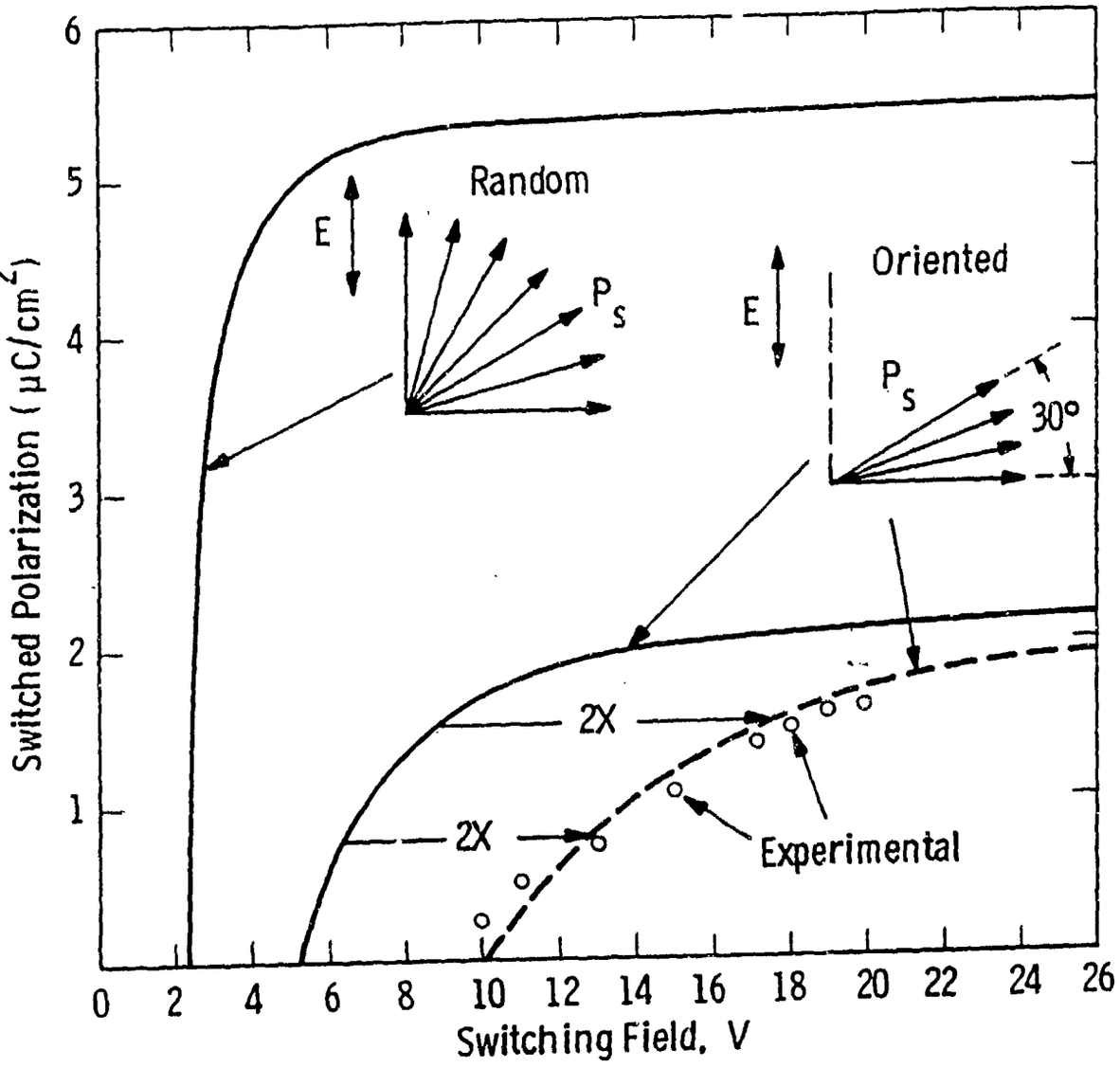


Figure 3-12: Polarization Switching Curves for BMF Films (2000 Å) Calculated From Single-Crystal Hysteresis Data.

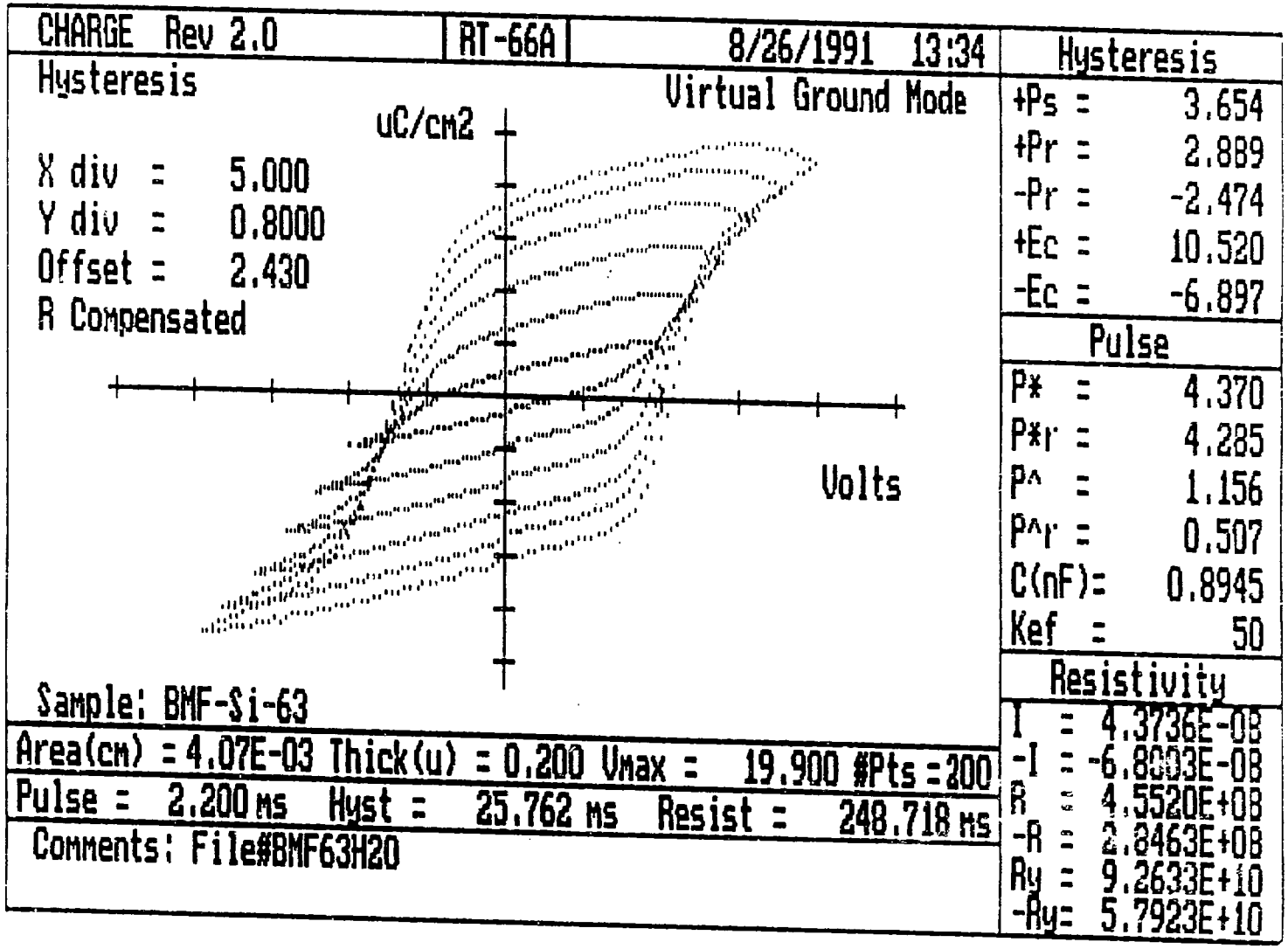


Figure 3-13: Family of Hysteresis Loops for BMF Film with Mainly Random Orientation and Weak (010) Fiber-Texture Second Phase

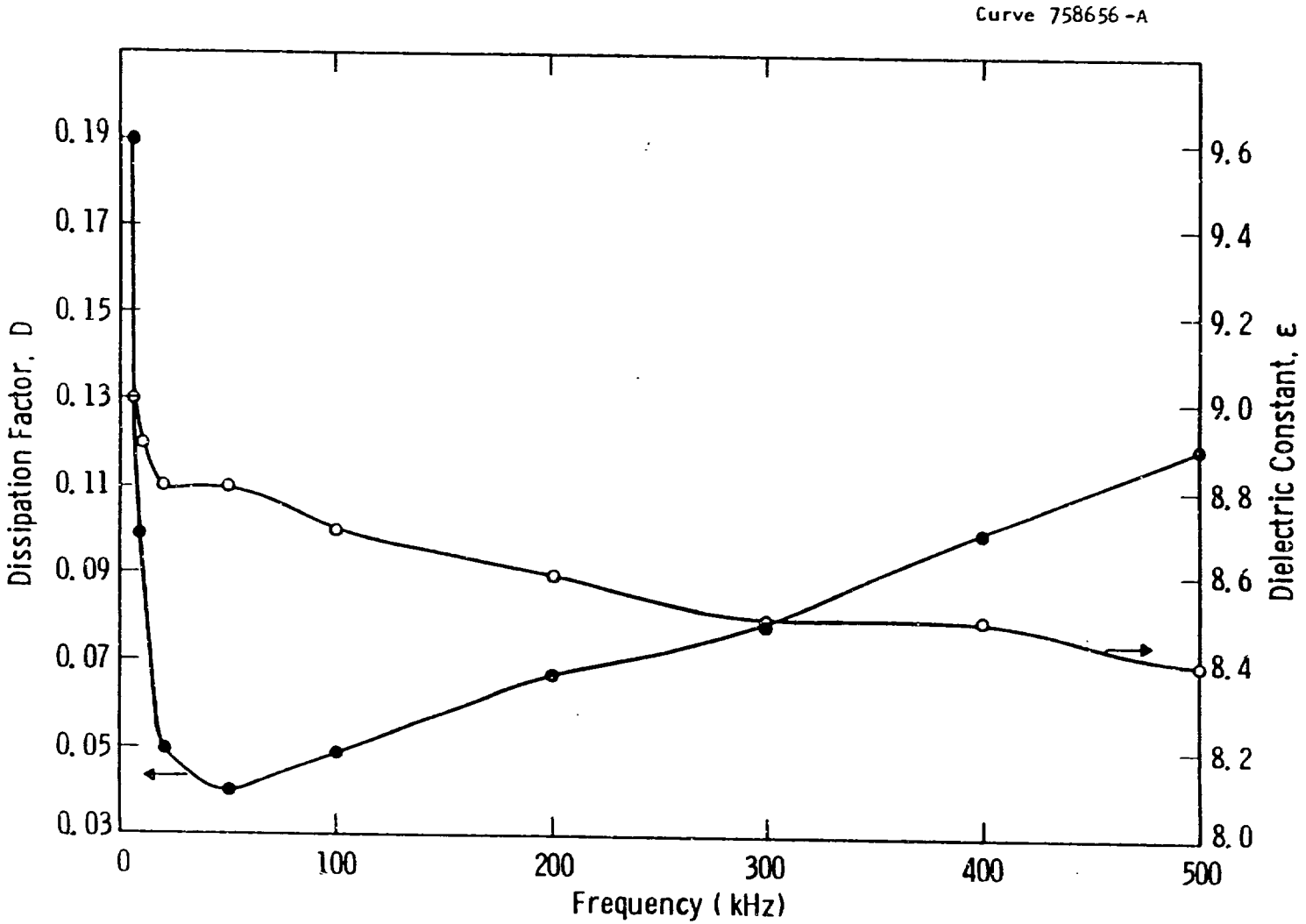


Figure 3-14: Dielectric Permittivity and Dissipation Factor For Fiber-Textured BMF Film Grown On Silicon

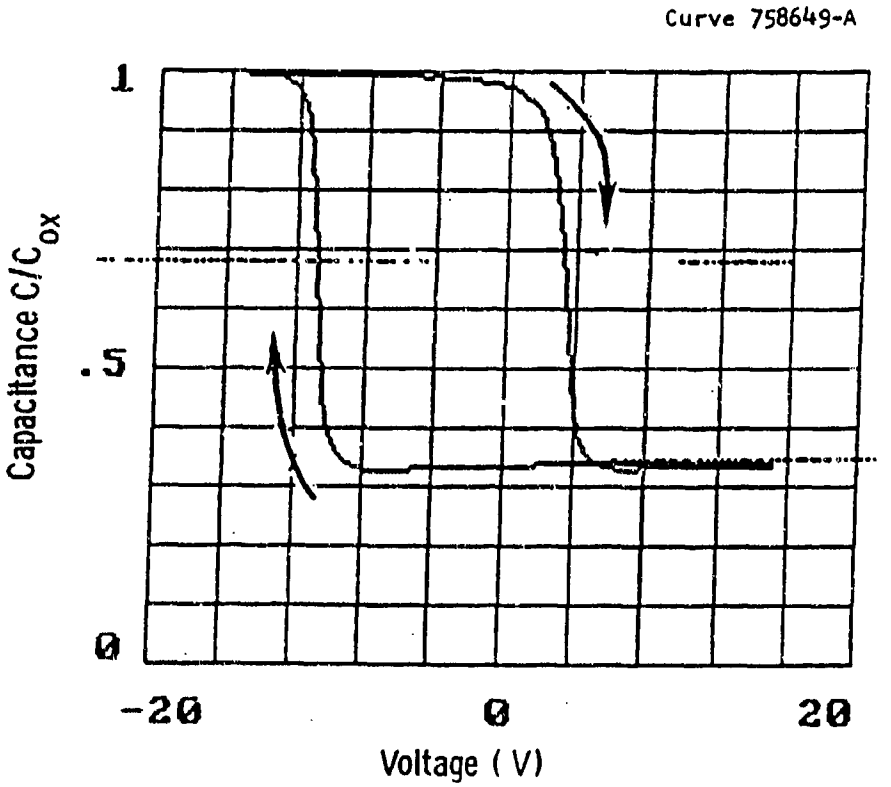


Figure 3-15: C-V Hysteresis Loop of 200nm BMF Film on Si(100). Threshold Voltage Shift of 14V. (Memory Window) from ±20 Volt Programming.

It should be pointed out that the evidence of ferroelectric switching, and the associated large memory window shown in the C-V plot of Figure 3-15, appear to be anomalous in view of the multiple epitaxial orientation of this film. This orientation would indicate that essentially no component of the ferroelectric polarization lies perpendicular to the film surface. However, the value of the voltage threshold shift in fact suggests that a polarization at least of magnitude 0.2 $\mu C/cm^2$ is being switched. This may be accounted for by regions of the film which are imperfectly epitaxially oriented, ($\approx \pm 30°$ out of the plane of the film) as illustrated in Figure 3-12.

3.4.2.2 Films With Dielectric Capping Layers

In the case of BMF films, the experimental results developed during this part of the program convincingly demonstrated the need to incorporate high-quality capping layers for several reasons. Ideally, we would seek to avoid the use of such layers, since they require higher programming voltages. However, the high temperatures used for some steps in IC processing, coupled with the extreme sensitivity of devices to impurities, mandated that the processes themselves should be protected from decomposition products possibly emitted from the fluoride films. The capping layer provides better memory gate adhesion and facilitates memory-gate stack photoengraving. Also, as discussed later, we strongly suspect that the tendency for many fluoride films to display high electrical leakage arises from thermal cracking of the film (and subsequent upper electrode penetration), resulting from the large differential expansion relative to the silicon substrate. To reduce these problems, a low-temperature CVD SiO_2 capping layer was applied to the fluoride film prior to further device processing steps. (Actually, the method of application chosen may introduce other unwanted degradation effects, and we return to discussion of this aspect later.) Several techniques were explored for deposition of SiO_2 capping layers on BMF films (on silicon) after they had been annealed at various temperatures. Most of the data were taken on films which had been furnace-annealed in hydrogen at 480°C. The capping growth techniques included rf-sputtering, plasma-enhanced CVD, remote-plasma CVD, e-beam evaporation, and low temperature CVD. The capping film results obtained by the first three methods invariably exhibited high electrical leakage. The SiO_2 layers produced by LPCVD (decomposition of silane and water vapor at about 400°C) were generally of excellent quality, displaying breakdown voltages in the range of 10^7 V/cm. Application of 50 nm LPCVD capping layers to 250 nm BMF layers, usually enabled test voltages up to 90 Volts to be applied to the resulting structure before breakdown occurred. Our previous observations of high leakage in uncapped films suggest that the cap in this situation is sustaining a field of at least 10^7 V/cm. Little or no polarization can be switched in uncapped films before breakdown occurs, and this usually happens at rather low voltages. In the case of capped films, typically a hysteresis loop began to form and opened as the voltage exceeded 30 V. When 90 V was reached a well-developed loop was recorded (Figure 3-16) indicating a P_S value of about 5 $\mu C/cm^2$, P_r = 3.5 $\mu C/cm^2$, and E_c = 44 V (1760 KV/cm). Note that P_S in the RT-66 nomenclature of Figure 3-16 stands for saturation polarization, whereas in this text, we have used P_S to denote spontaneous polarization. The actual voltage across the fluoride close to breakdown can be estimated from the capacitances of the oxide and fluoride layers. The fact that C_{ox}/C_F = 2/1 indicates that two thirds of the applied voltage (i.e. about 60 V) is across the fluoride, and that the true value of E_c should be about 1060 KV/cm. The voltage sustained by the fluoride in the capped structure is apparently more than twice as great as the voltage causing breakdown in the uncapped structure.

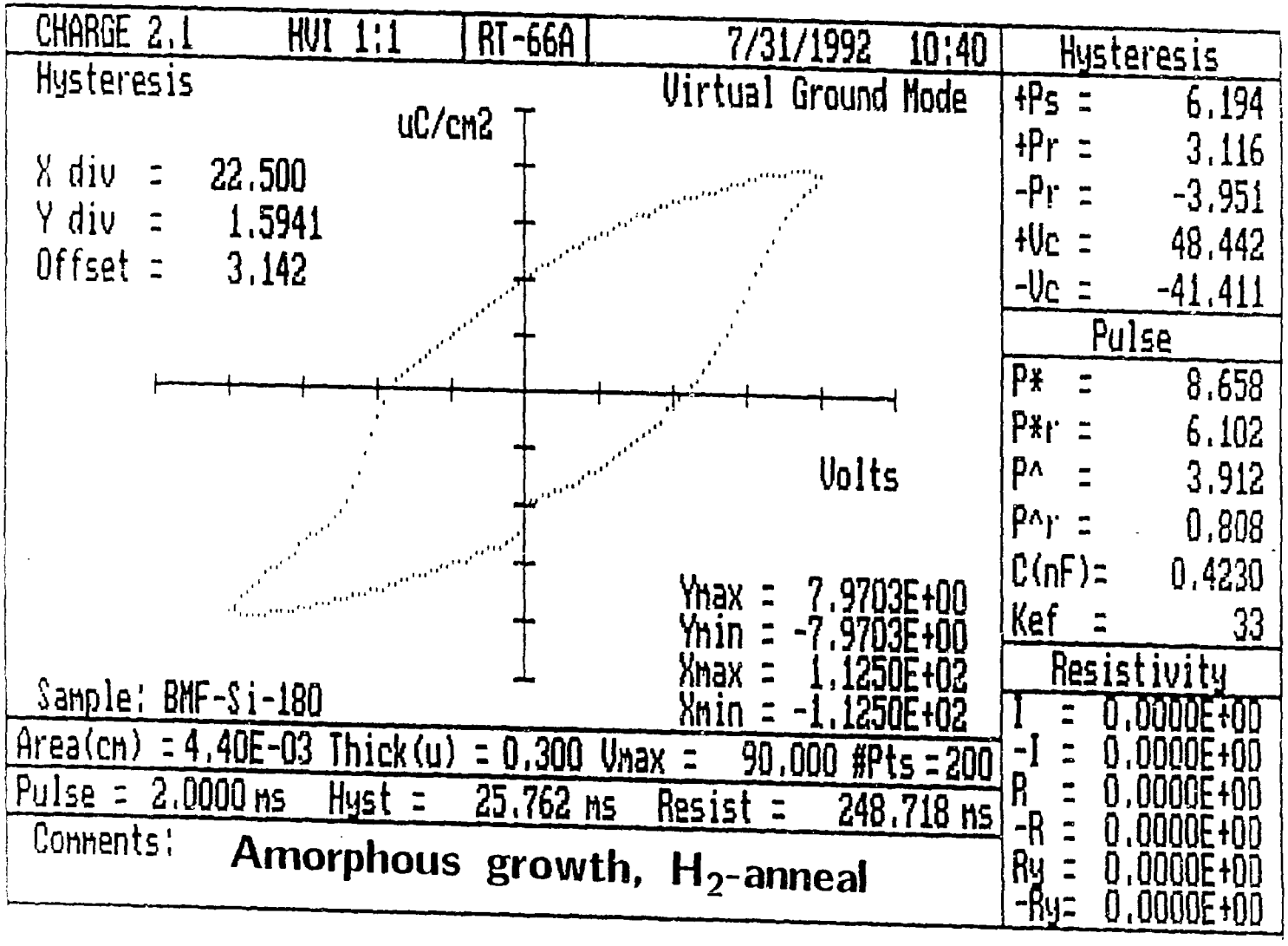


Figure 3-16: Hysteresis Loop For Capped BMF Film

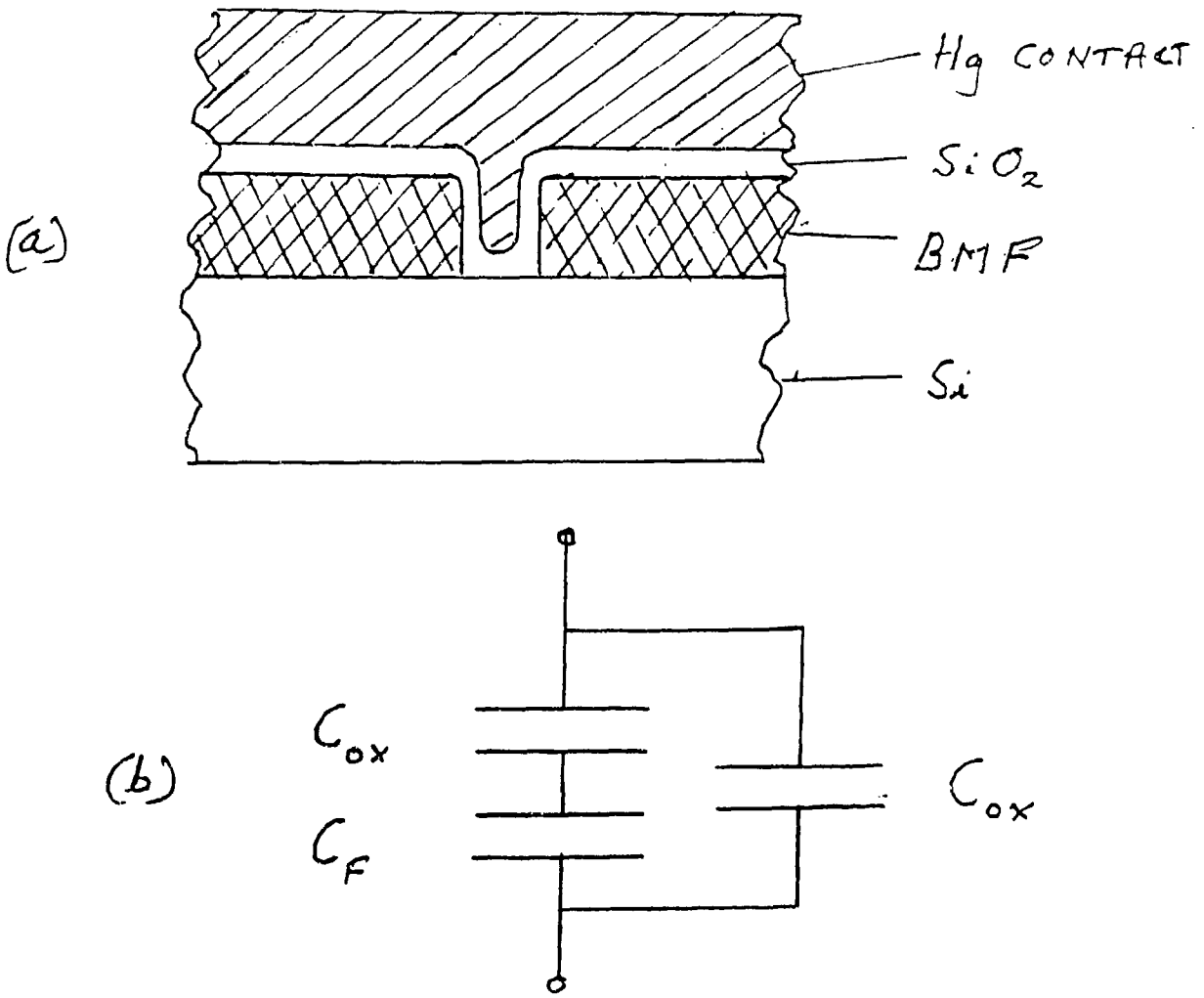


Figure 3-17: Suggested Structure and Equivalent Circuit for Capped BMF Layers, Showing Effect of Oxide Cap in Sealing Cracks in the Fluoride Film.

The dramatic change in behavior after application of the cap leads us to suggest a structure and equivalent circuit model of the type shown in Figure 3-17. We propose that intergranular leakage is blocked by the high-quality oxide cap layer which penetrates into and seals the cracks. For the 90 V applied voltage indicated in Figure 3-16, the 50 nm intergranular oxide cap would be sustaining a field of about 2 X 10^7 V/cm. The field in the oxide cap overlying the fluoride would be about one third of this value. It is obvious from these data, that the fluoride layer, at least in uncracked regions, must be capable of withstanding effective fields high enough to allow ferroelectric switching; otherwise the loop results depicted in Figure 3-16 could not have been obtained. Capped BMF films with Aluminum dot top electrodes exhibited C-V memory windows that often exceeded the programming voltage. A typical example is shown in Figure 3-18, where the test structure cross-section on a gridded silicon wafer is shown on the left hand side. Notice the 21 V memory window obtained with 16 V programming. This film was grown at 200°C and then annealed in forming gas at 480°C for 60 minutes. A ferroelectric hysteresis plot obtained with the same sample at 30 Hz using our modified Sawyer-Tower bridge is shown at the bottom right hand side of Figure 3-18. Ferroelectric switching speed of this film (with the same test structure) was measured at Penn State

University by Prof. Krupanidhi. The experimental set up was identical to the one used by Larsen et al.[15] for the measurement of ferroelectric switching speed of PZT films. The results shown in Figure 3-19 (difference curve of the voltage transients between a switching pulse followed immediately by a non-switching pulse) indicate that the ferroelectric polarization reversal time for the BMF film was in the range of 40 to 45 nanoseconds. Thus the BMF films treated in the manner described above do possess the required fast switching speed for FEMFET application.

Fatigue measurements were also performed on BMF films using a RT-66A test system. Typical endurance/fatigue test results (obtained with the same BMF film and test structure for which the C-V, hysteresis, and switching speed results were shown in Figures 3-19 and 3-20) showed only a 22% reduction in the remanent polarization (P^*_r) after 2.9×10^9 switching cycles at 60 V, as shown in Figure 3-20 (limited by continuous test-equipment use-time). Retention experiments performed on the same film with the same test structure using the RT-66A test system showed no measurable loss of remanent polarization after 4.4×10^5 seconds. Since significant loss of retention was observed with BMF films in the transistor configuration (described in detail in Section 3.7), the retention experiments were repeated with a BMF film (with a 13.5 nm thermal SiO_2 buffer between the BMF and the Si substrate) that was grown at 200°C and then annealed in forming gas for 60 minutes. The film was capped with LPCVD SiO_2 and Al-dot patterned at ATL, where it exhibited excellent C-V characteristics, but poor retention in the transistor configuration, because of the threshold drift after programming. With the RT-66A system, the same test structure exhibited a good ferroelectric hysteresis loop at 80 V, as shown in Figure 3-21. Retention experiments were performed for a cumulative 8.6×10^5 seconds, first with V_{wr}=-80V, V_{rd}=80V (Figure 3-22), and then with V_{wr}=80V, V_{rd}=80V (Figure 3-23). The difference plot is shown in Figure 3-24. The hysteresis loop following the completion of the retention experiment is shown in Figure 3-25. It is clear from Figure 3-24, that the +/+ "Null" difference is stable during this period; but the -/+ Remanent polarization decays, eventually even through "Zero".

It is evident from the hysteresis results shown in Figure 3-16 and from the circuit model in Figure 3-17, that the memory windows observed for these capped films are being produced by very small actual values of switched polarization (since the effective voltage across the fluoride film is probably less than 12 to 14 V). Under such conditions, at these small charge levels, reverse switching could readily occur under the influence of internal fields generated by stress effects. Studies made on our BMF films by Prof. Seshu Desu and his group at Virginia Polytechnic Institute and State University have revealed that such high stresses are indeed present after heat treatments of the type used for our samples (see Figures 3-6 and 3-7). Although drawing further conclusions concerning long-term retention of charge at the semiconductor/BMF film interface from the above experiments is difficult, it may be possible to reduce both intergranular and intrinsic leakage by changing the procedure used for thermal crystallization of the BMF films, and perhaps by modifying the process for applying capping layers.

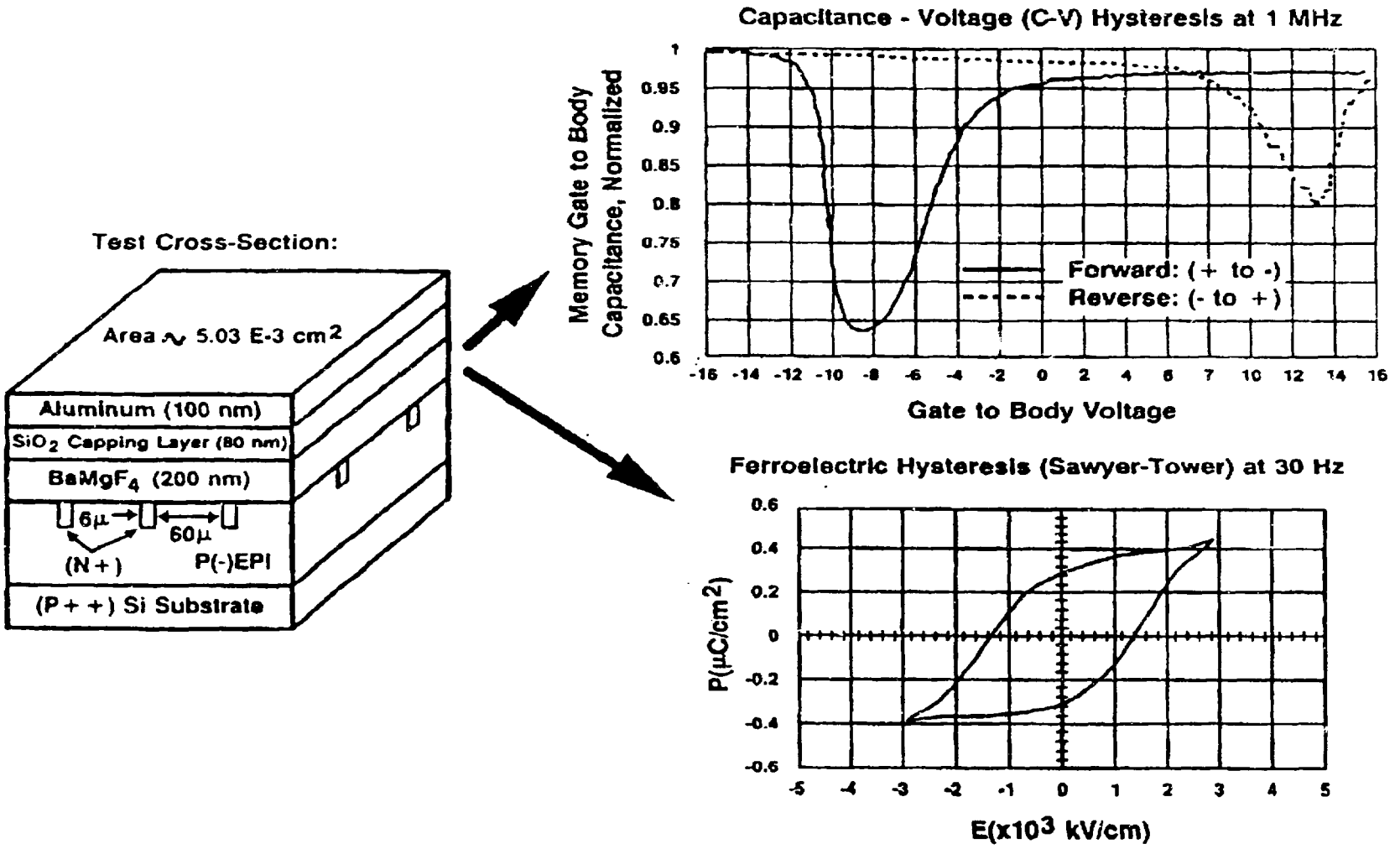


Figure 3-18: Typical Hysteresis Curves Measured On A Capped BMF Film with Al-dot Top Electrode

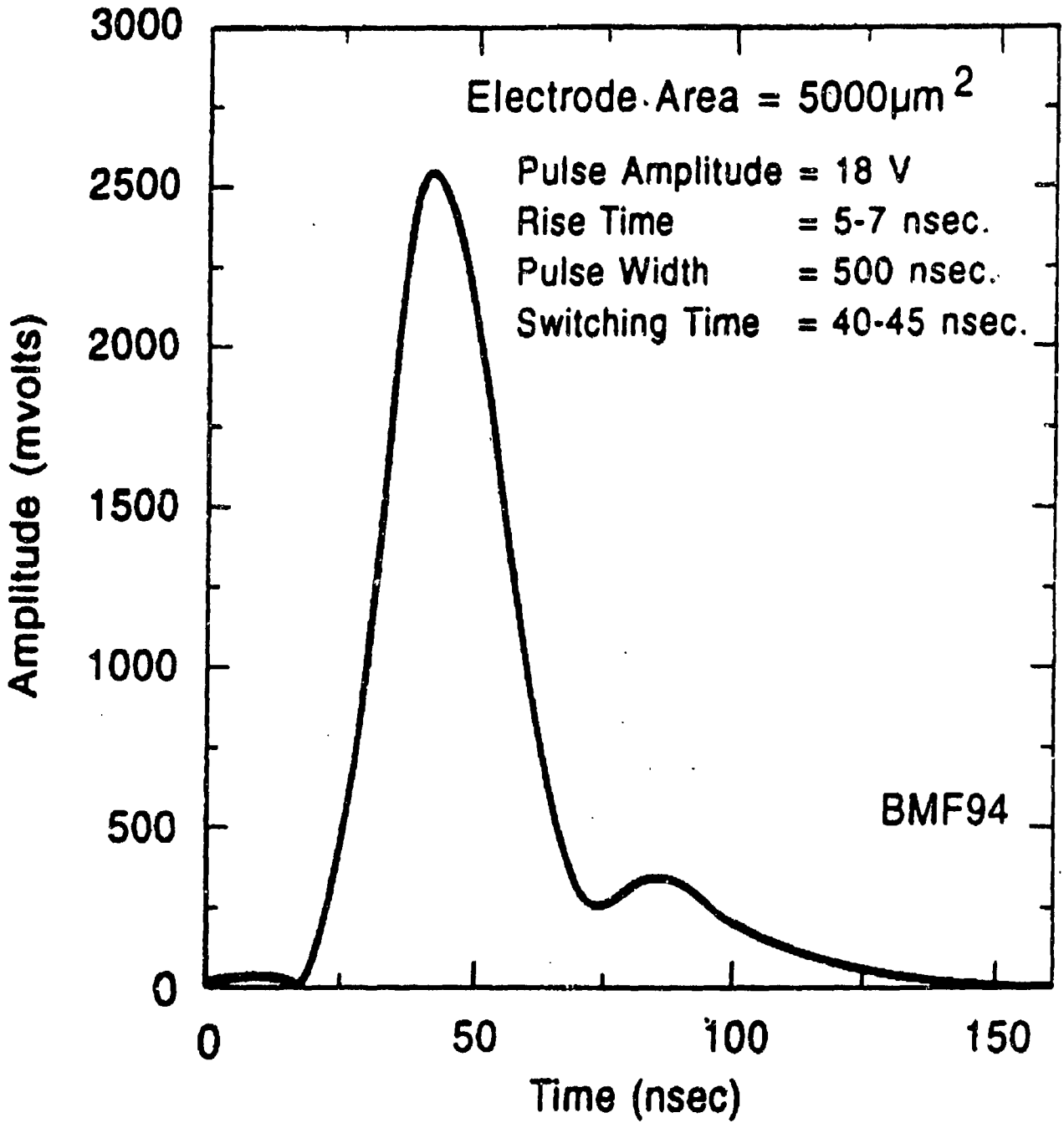


Figure 3-19: Pulsed Polarization Reversal Switching in BMF Thin Film (measured by Professor Krupanidhi, Penn State University)

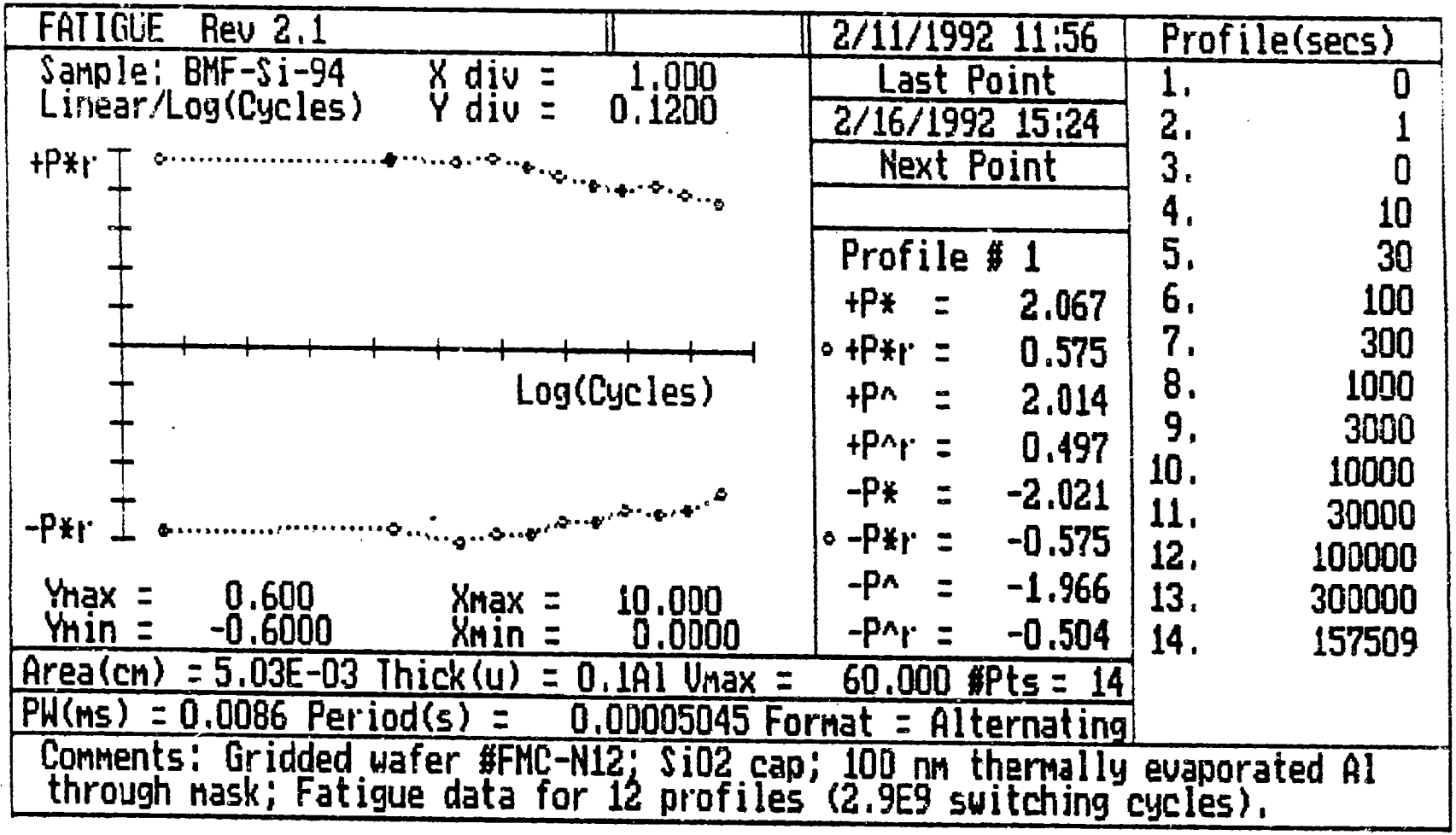


Figure 3-20: Typical Endurance/Fatigue Test Results for BMF Fiim with Al-dot Top Electrode

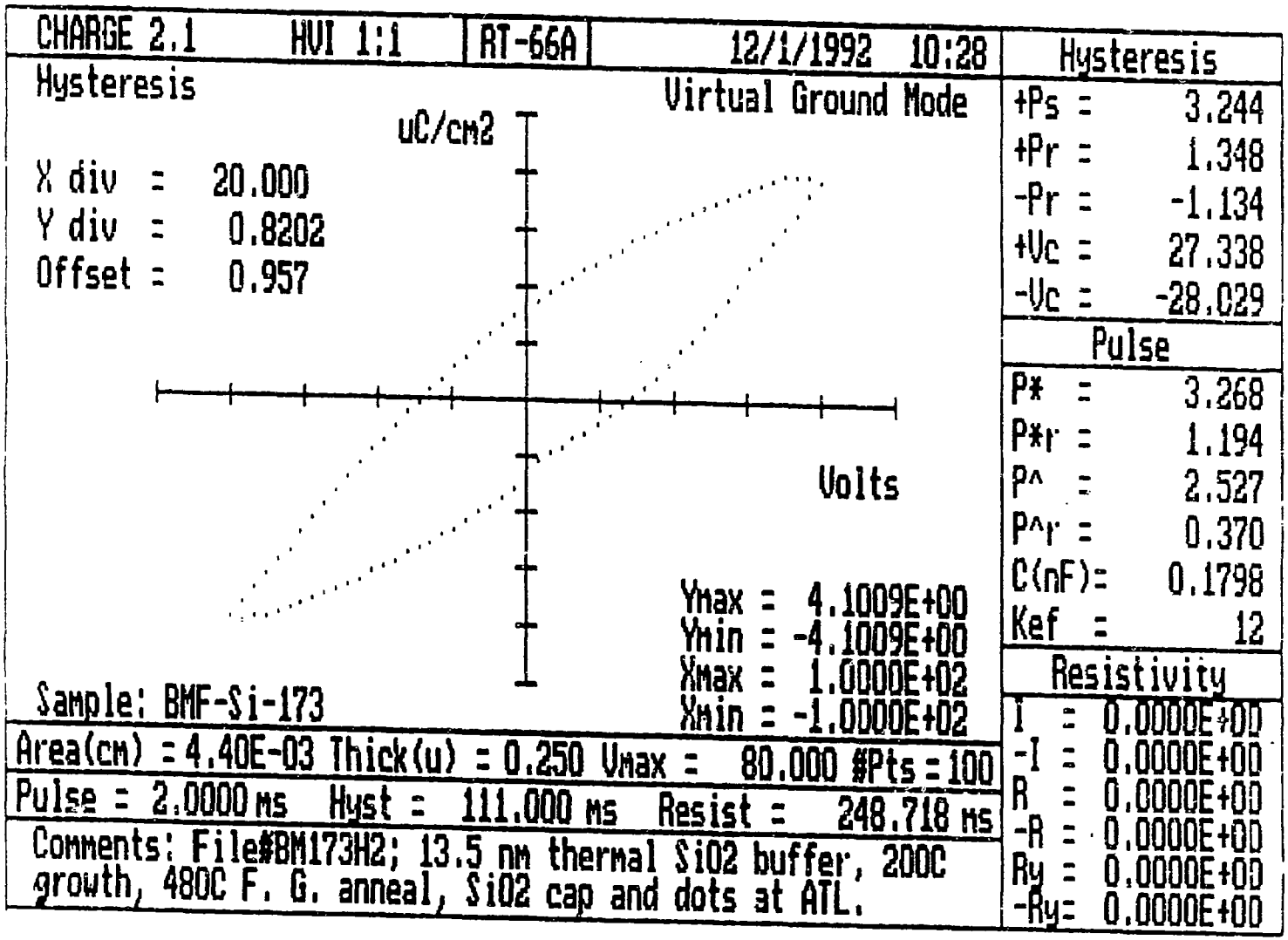


Figure 3-21: Ferroelectric (BMF173) Hysteresis Loop on RT-66A System

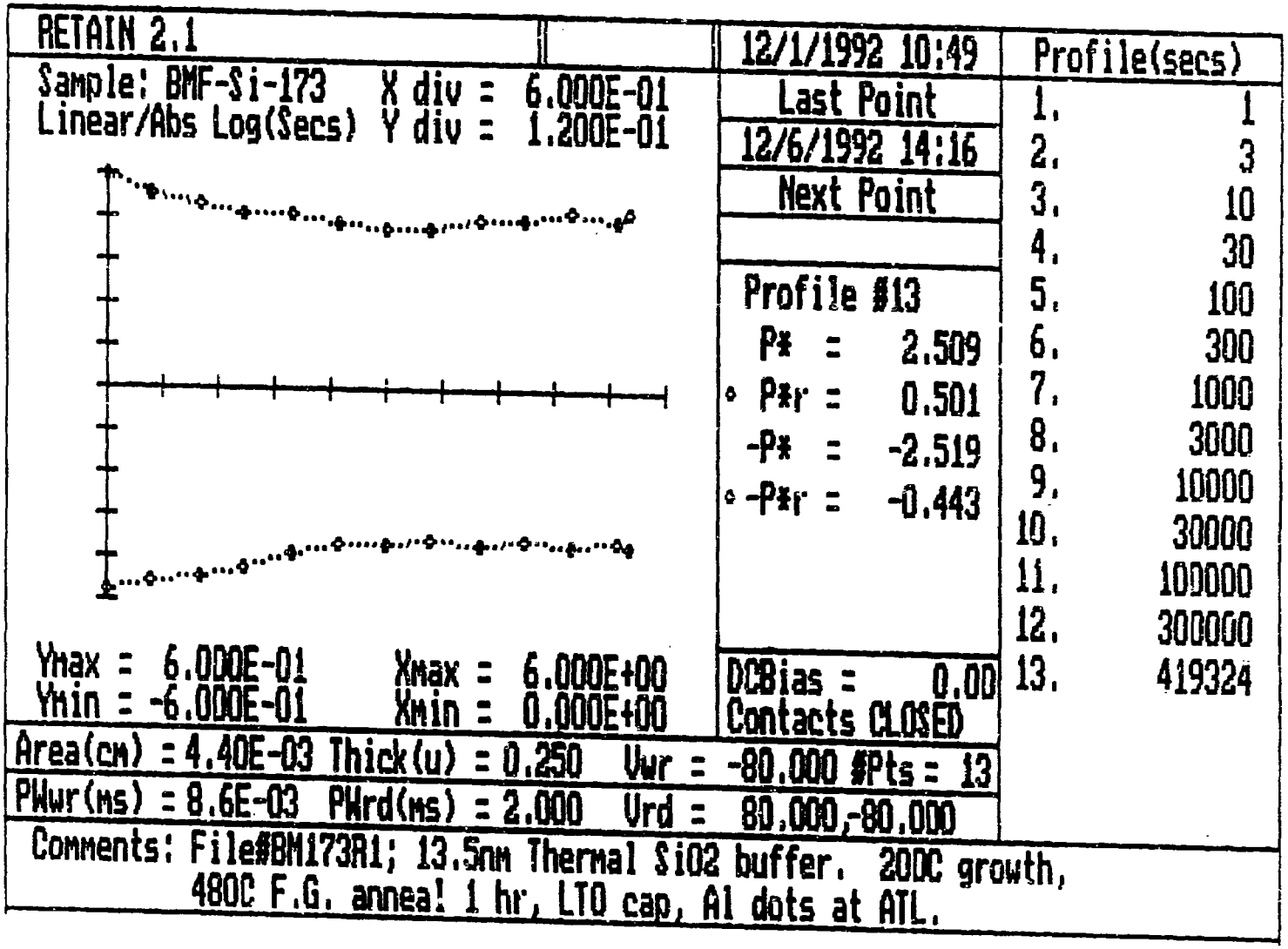


Figure 3-22: Retention (V_{wr} = -80V, V_{rd} = ±80V) Results for BMF173

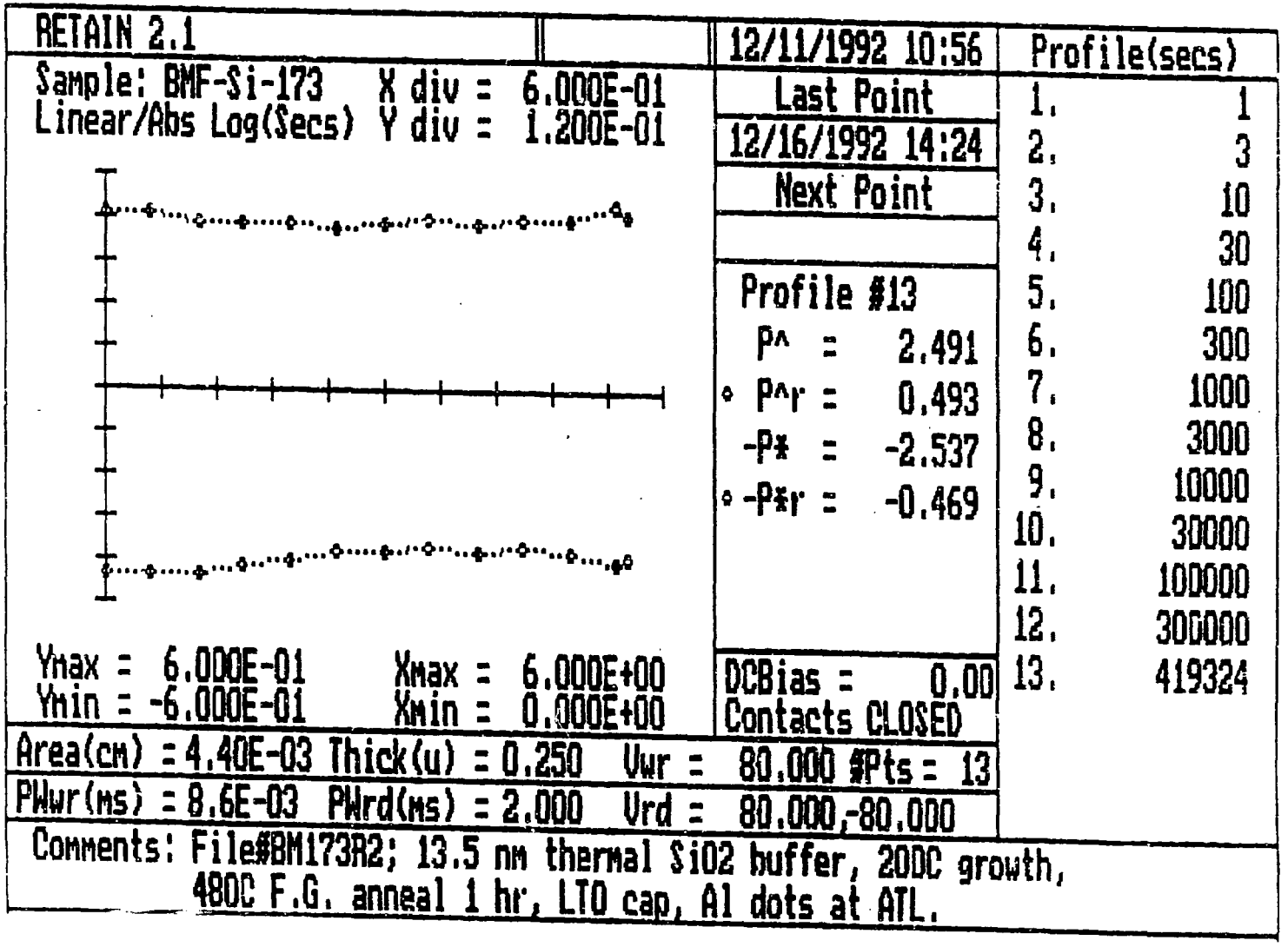


Figure 3-23: Retention (V_{wr} = 80V, V_{rd} = ±80V) Results for BMF173

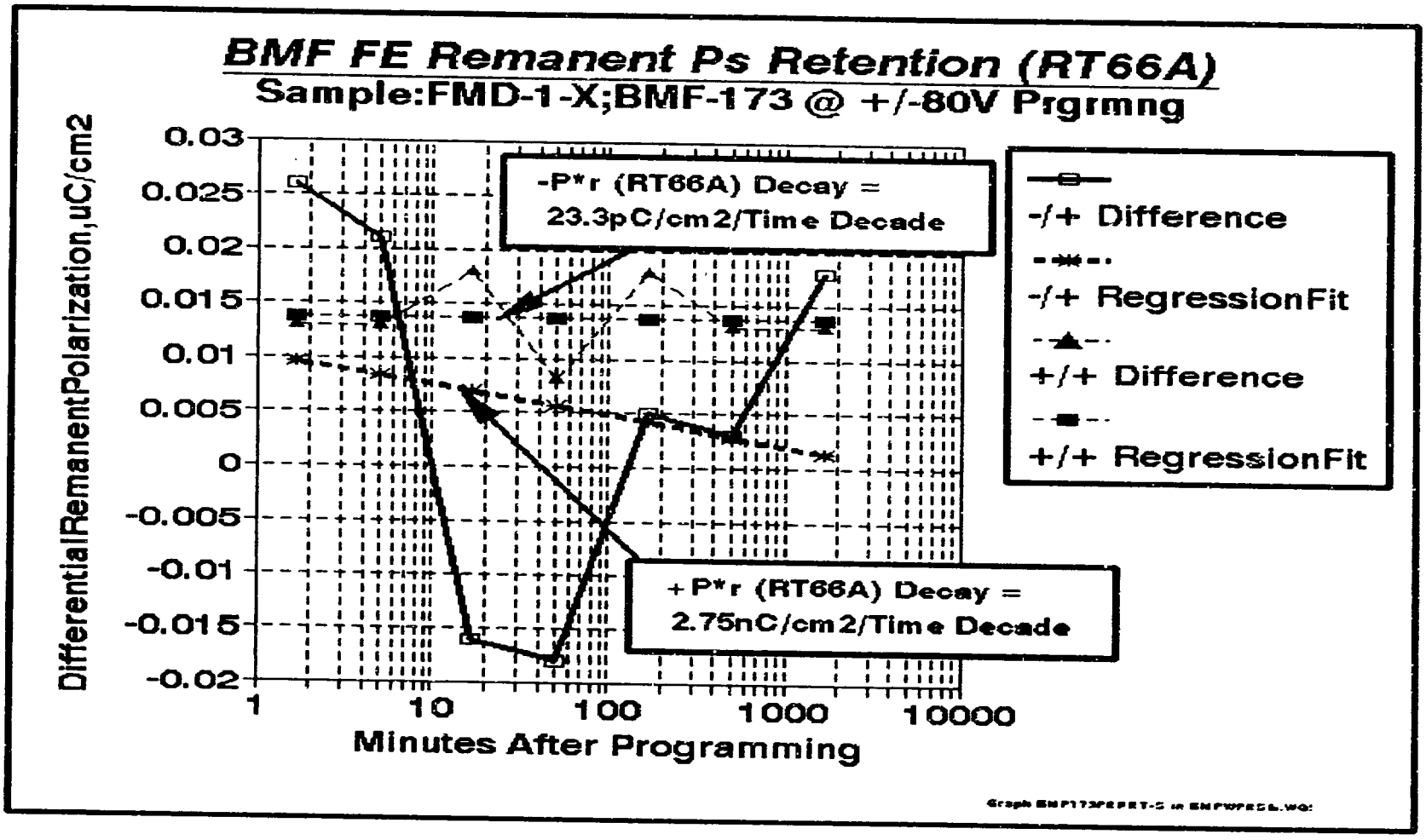


Figure 3-24: Usable Retention Difference Results for BMF173

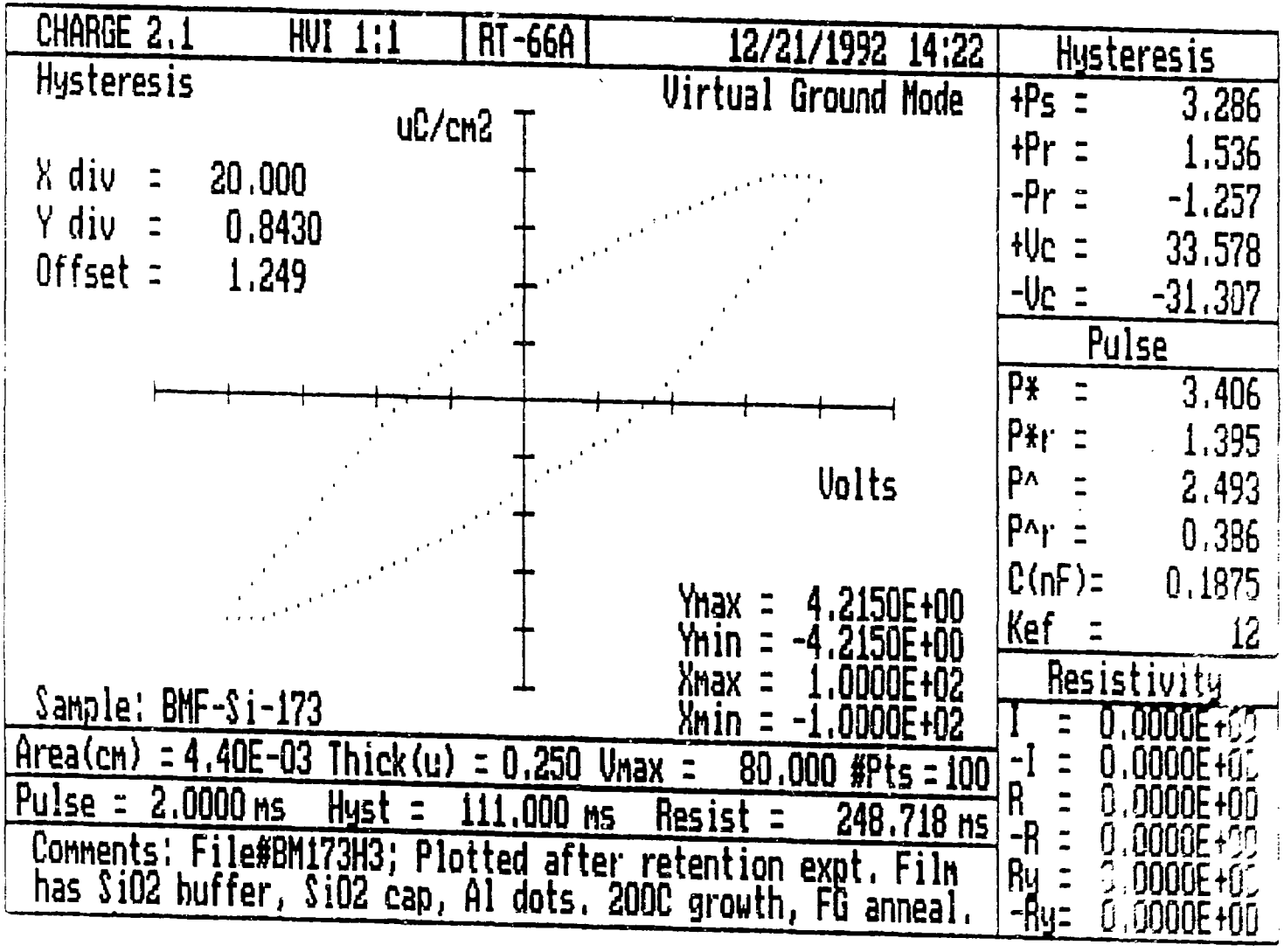


Figure 3-25: Hysteresis Loop After Retention Tests.

3.5 8K FERRAM Test Vehicle

An 8K FERRAM Test Vehicle was created for evaluation of FEMFET baseline process integrity. This test vehicle was created by modifying an existing 4 um test vehicle from a Westinghouse/Sandia National Laboratories 8K EEPROM program. This program employed a SONOS (Silicon Oxide Nitride Oxide Semiconductor) nonvolatile memory transistor approach. The Westinghouse FEMFET baseline process was designed to be compatible with this SONOS technology.

A detailed description of the 8K FERRAM Test Vehicle is included in Appendix C. Included in this description are:

- Mask design rules
- FEMFET cross section
- Mask polarity information
- Mask alignment sequence/tolerances
- Wafer map
- Test structure description/probe pad information
- Plots of test structures

1X projection print photolithography was used for the FEMFET process. This allowed multiple devices to be placed on each FEMFET wafer. The 8K FERRAM Test Vehicle maskset was comprised of the following devices:

Device	# per wafer
- 8K FERRAM EEPROM	62
- WEC Process Test Pattern	56
- SNL Process Test Pattern	56
- SNL Self Stress Test Pattern	6
Total die =	180

This maskset featured a full complement of test structures for evaluation of the process integrity of the FEMFET process. These test structures addressed such issues as performance, reliability, producibility, radiation hardness, and uniformity of the baseline technology. The key test structures were:

- CMOS transistors of varying widths and lengths
- FEMFET transistors of varying widths and lengths
- Gated diodes
- Metal contact structures
- Sheet resistivity test structures
- Field parasitic MOSFETs
- Area capacitors
- SCR test structures

The 8K FERRAM was designed using a four transistor memory cell. Each memory cell has two FEMFET memory transistors and two NMOS access transistors. The dual memory transistor approach results in a

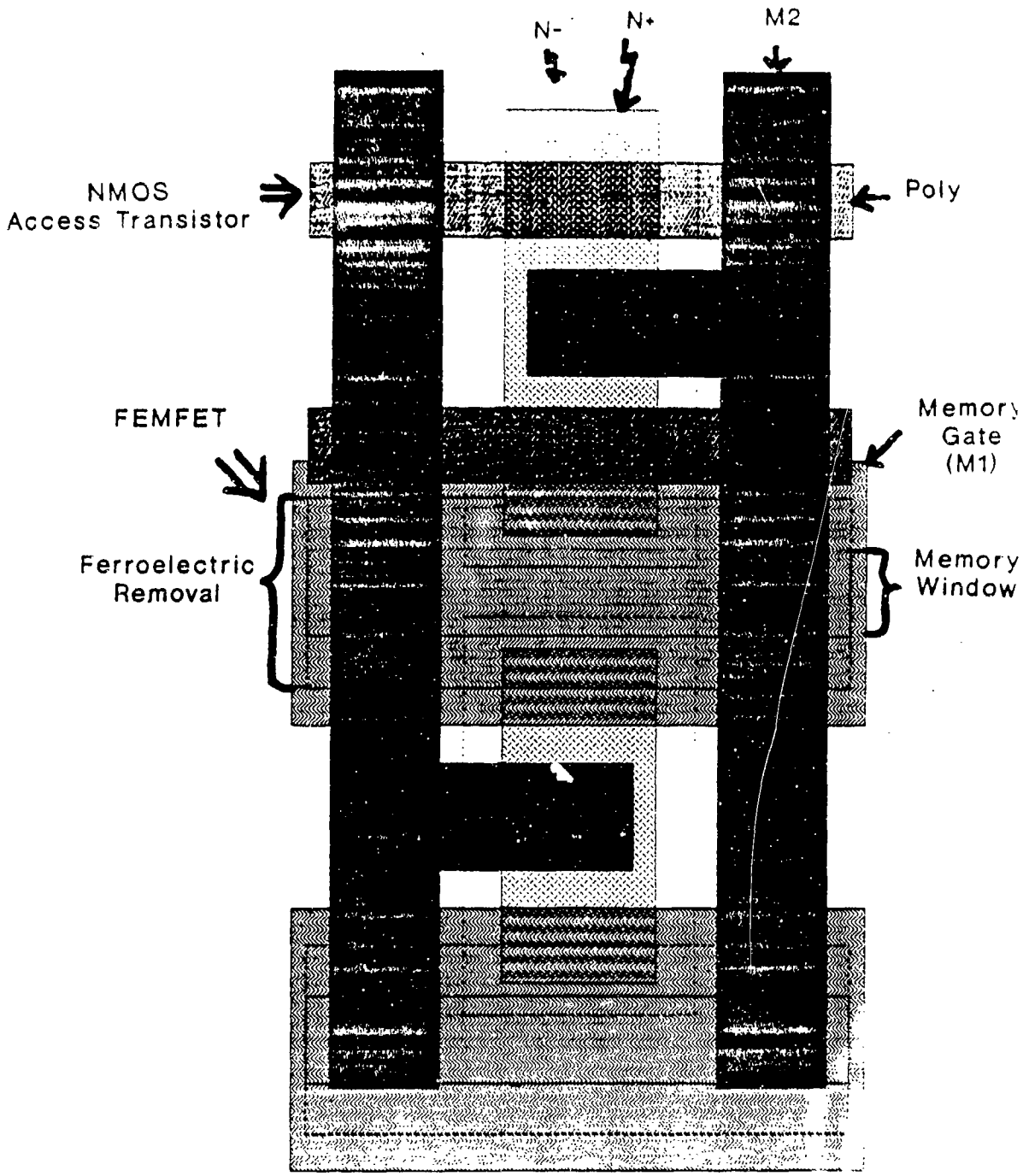


Figure 3-26: 8K FERRAM Memory Cell

much more robust design and is commonly used in military nonvolatile memory applications. Differential sense amplifiers are used which can detect differences in memory transistor threshold voltages as small as 50 mV. Figure 3-26 shows a plot of the FERRAM memory cell. This cell has dimensions of 40 um x 60 um. Design rules were selected to maximize the producibility of the FEMFET. The general approach selected was to make design rules as conservative as possible to allow for flexibility in processing. This approach allowed a wider tolerance for wet versus dry chemistry processing. The resulting memory cell could then be used as a demonstration vehicle for a wide range of ferroelectric materials. The plan for this phase of the program was to demonstrate a FEMFET process suitable for military nonvolatile memory applications. Upon successful completion of this task, design rules would be evolved to allow for high density memories in the future.

Based on a detailed process review, the following changes to the original 4 μm memory cell were instituted which should result in significant improvements in producibility and memory transistor drain breakdown. These changes were:

1. Memory gate metal overlaps all ferroelectric material to allow the baseline VHSIC metal etch to be done. By overlapping the ferroelectric memory gate over the ferroelectric stack, the ferroelectric should be completely shielded from attack during the baseline M1 etch. This should avoid some of the more complicated approaches considered for this step. The ferroelectric removal mask overlaps memory window by 2.7 μm (0.5 μm single misalignment tolerance, 1.0 μm MW etch, 0.25 μm ferroelectric stack etch, plus 0.95 μm safety - 2.7 μm). [This was achieved by reducing the MW overlap of N- extender from 1.7 μm to 1.0 μm.] This is needed to ensure that no bare silicon exists inside memory window when memory gate is deposited. In order to guarantee that memory gate (M1) overlaps the ferroelectric stack, a design rule of 1.9 μm was selected for M1 overlap of the stack (0 μm for ferroelectric stack etch, 1.0 μm for 4 misalignment tolerances, plus 0.9 μm safety - 1.9 μm). This results in a minimum M1 spacing of 2.0 μm in the memory array, which is approved for projection printing at ATL.

2. N- extender overlaps N+ extender in all directions to increase memory transistor drain breakdown from roughly 17V to 22-24V. This should allow the FEMFETs to be characterized at 20V. The ferroelectric memory transistors were modified so that the N- extender overlaps the N+ source-drain in all directions by 2.0 μm. (For the Sandia 4 μm design, it presently only overlaps the N+ in the channel region.) This will eliminate breakdown problems associated with the edge of the N+ drains. This change increases the FEMFET effective width from 8.0 to 12.0 μm. This also reduces the N- to P+ guardband space from 8.0 to 6.0 μm.

3.6 BMF FEMFET Baseline Process Description

Wafer fabrication on this program used short-loop gridded wafers for ferroelectric capacitor fabrication and fully processed device wafers for FEMFET fabrication. During this program phase, 150 gridded wafers and 18 device wafers were completed. In addition, 37 device wafers were processed up to FEMFET formation and were held pending results from gridded wafer tests.

Gridded wafers consisted of P on P+ starting wafers with an orthogonal grid of 6 um wide N+ diffusions at 100 um spacing. These N+ grids provide a source of minority carriers during electrical testing and result

in more accurate evaluation of ferroelectric film properties. The gridded wafers were used as an effective tool for evaluating suitability of various ferroelectric films for FEMFET fabrication. Ferroelectric dielectrics were first deposited on these gridded wafers for capacitance-voltage (CV) electrical evaluation. These measurements provided a rapid assessment of important ferroelectric properties such as memory window size, position, endurance and retention. Typical throughput time for these wafers was about 1-2 weeks. This allowed for rapid optimization of various deposition parameters such as:

thickness, anneal temperature, and deposition ambient.

Upon successful completion of gridded CV tests, ferroelectric films were selected for use on fully processed device wafers. These device wafers were processed with a 4 um dual well CMOS process developed for Sandia National Laboratories for their SONOS 8K EEPROM fabrication. The design rules for that EEPROM formed the basis of the design rules for the 6083 8K FERRAM test vehicle and are given in Table 3-6. The Sandia EEPROM SONOS process was modified such that the FEMFET transistor would replace the SONOS memory transistor in this design. A baseline process was selected at the beginning of the program with the following objectives:

- minimization of high temperature operations
- processes compatible with VLSI double metal processing
- processes must not risk fab line contamination
- design rules compatible with dry or wet chemistry

The FEMFET baseline process cross section and process flow are shown in Figure 3-27 and Table 3-7. The ferroelectric memory transistor steps are highlighted in bold text. The key process elements for FEMFET transistor fabrication involved:

- memory window formation
- ferroelectric deposition and etch
- memory gate deposition and etch

The FEMFET processing was incorporated as the last processing steps prior to first metallization in order to minimize the number of high temperature cycles to which the ferroelectric material was exposed. The FERRAM process adds two additional masks to a conventional CMOS process in order to define FEMFET memory transistors. Since two additional masks are also required to make SONOS devices, both technologies require 16 masks.

TABLE 3-6: Design Rules for the 6083 8K NDRO FERRAM ICAL Test Vehicle

Level		Design Rule	
#	Name	Feature / Item	Value, μm
7	N-	+ Overlap of memory gate/M1 + Minimum space (channel length)	> 0.7 > 2.6
8	N+	+ Space to MG/M1	> 1
10	Contact	+ Minimum contact + Space to memory window	3 x 3 (2.5 x 2.5 on Mask) > 4
11	Memory Window	+ Overlap of MG/M1	> 1
12	Ferroelectric Removal	+ Overlap of M W	> 2
13	Memory Gate/M1 (MG/M1)	+Minimum width + Minimum space + Overlap of Contact	4 (5.6 on mask) 4 (2.4 on Mask) 0.5 (1.55 on Mask)
14	Via	+ Minimum via	3 x 3 (2.5 x 2.5 on Mask)
15	M2	+ Minimum width + Minimum space + Overlap of via	4 (5.6 on mask) 4 (2.4 on mask) 0.5 (1.55 on masks)

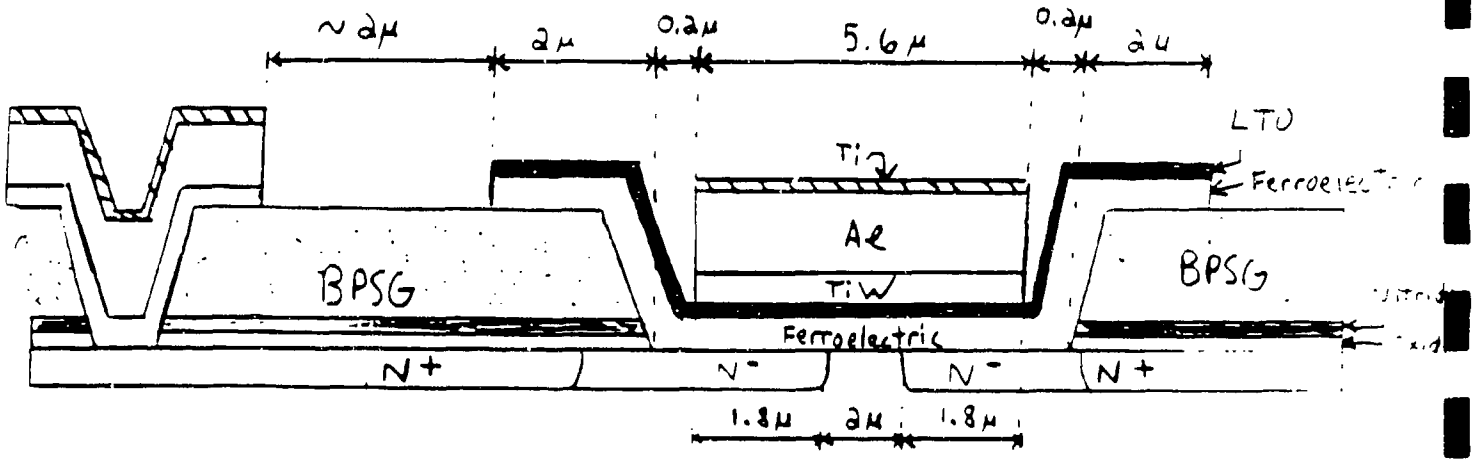


Figure 3-27: Westinghouse FEMFET Process Cross Section.

A series of unit process development experiments were conducted to optimize the processes selected for FEMFET fabrication. A memory window process was identified which allowed this window to be reflowed along with the normal contact window reflow. This approach resulted in near ideal contour of the FEMFET memory window, eliminating any subsequent concerns about metal step coverage.

Figure 3-28 is a SEM of reflowed memory window and shows that the process provides a smooth profile for good metal step coverage. Figure 3-29 is a SEM of a BMF FEMFET after first metal definition. With a baseline process established, ferroelectric FEMFET memory transistors were successfully demonstrated on BMF ferroelectric films. The next section will disucss the electrical measurements on these devices.

TABLE 3-7: FEMFET Baseline Process Flow.

Step #	Fabrication Process	Step #	Fabrication Process
1	Wafer issue	42	Phos. implant
2	Laser oxide	43	Resist strip
3	Laser #	44	N+ photo (8)
4	Strip oxide	45	Phos. implant
5	Pad oxide	46	Resist strip
6	Alignment photo (0)	47	P+ photo (9)
7	Oxide/silicon etch	48	Boron implant
8	Strip oxide	49	Resist strip
9	Pad oxide	50	Reoxidation
10	N-well photo (1)	51	Nitride dep.
11	Phos. implant	52	BPSG dep.
12	Resist strip	53	Densification
13	P-well photo (2)	54	Contact photo (10)
14	Boron implant	55	Contact etch
15	Resist strip	56	Memory window photo (11)
16	Oxide strip	57	BPSG etch
17	P/N-well drive	58	Reflow
18	Oxide strip	59	Oxide etch
19	Pad oxide	--	(H2 anneal omitted)
20	N-guard band photo (3)	60	Platinum dep.
21	Phos. implant	61	Silicide anneal (Contacts silicide, MW not silicided)
22	Resist strip	62	Platinum strip
23	P-guard band photo (4)	* 63	Memory window photo (11)
24	Boron Implant	* 64	Nitride/oxide etch
25	Strip resist	* 65	Ferroelectric removal photo (12)
26	Strip oxide	* 66	LTO dep.
27	Pad oxide	* 67	Ferroelectric removal photo (12)
28	Nitride dep.	* 68	Ferroelectric etch
29	Device window photo (5)	69	First metal dep. (TiW/Al/Ti)
30	Nitride/oxide etch	70	M1 photo (13)
31	Field oxidation	71	M1 etch
32	Nitride/oxide	72	Sinter
33	Sac. oxide	73	BSQ dep.
34	Oxide strip	74	Via photo (14)
--	(SNOS steps omitted)	75	Sloped via etch
35	Gate oxide	76	M2 dep. (Ti/Al)
36	Poly dep.	77	M2 photo (15)
37	Poly dope	78	M2 etch
38	Poly photo (6)	79	Overcoat dep.
39	Poly etch	80	Overcoat photo (16)
40	Pad oxide	81	Overcoat etch
41	N-extender photo (7)	82	Sinter

* = Ferroelectric-Unique Process Steps Are Shaded.

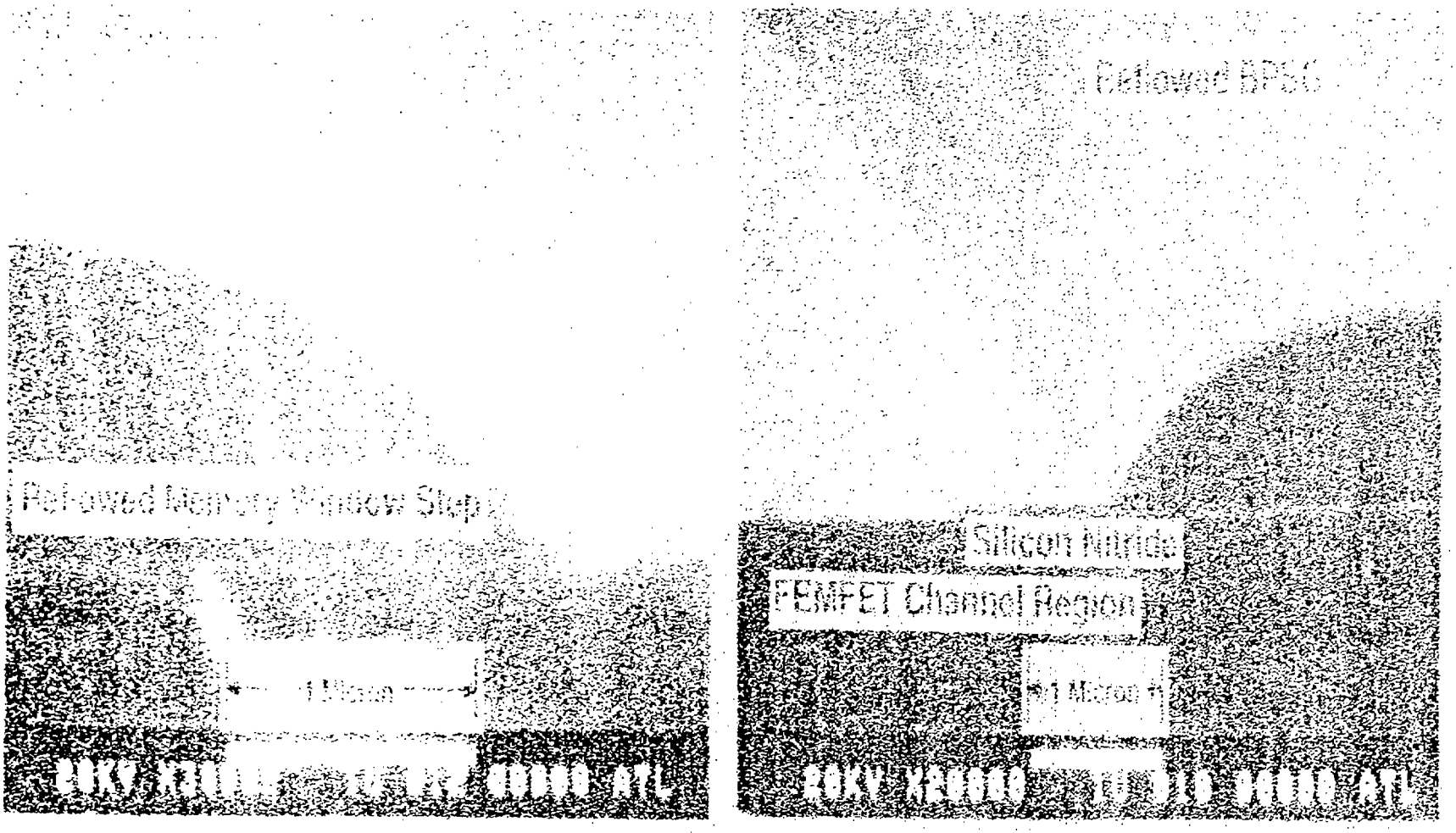


Figure 3-28: SEM of Reflowed Memory Window Shows Smooth Profile for Improved Metal Step Coverage.

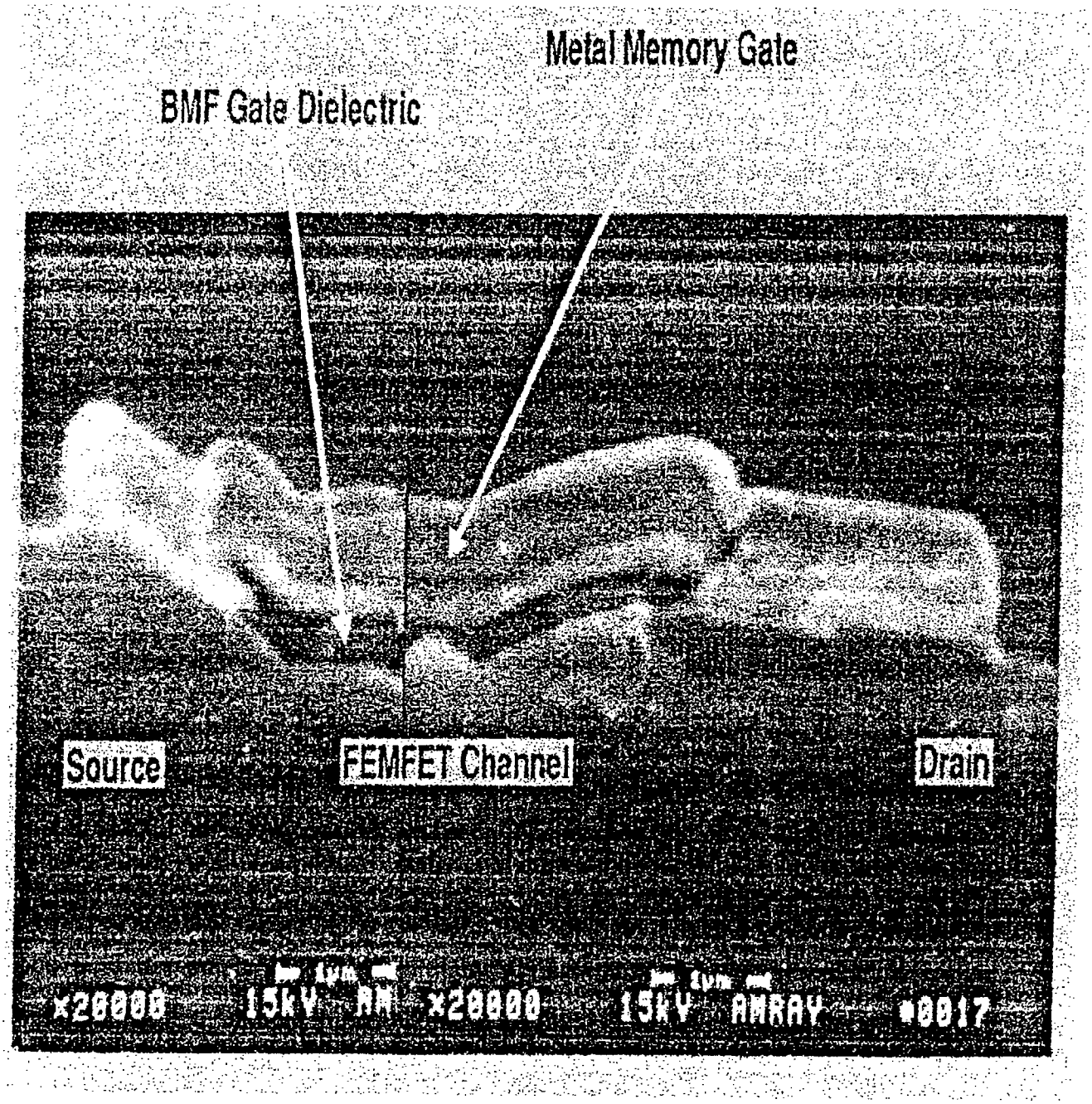


Figure 3-29: SEM of BMF FEMFET After First Metal Definition.

3.7 BMF-FEMFET Electrical Testing

Process optimization for such parameters as buffer oxide thickness, ferroelectric film thickness/growth ambient, capping oxide, film anneal, and metal composition/thickness was performed on short-loop gridded capacitors. Upon successful demonstration of ferroelectric CV behavior, FEMFET memory transistors were fabricated. This section will discuss the key electrical test results from the BMF FEMFETs that were produced. A total of 14 device wafers were processed. Table 3-8 summarizes the key parameters evaluated on these device wafers. Most wafers were processed through first metal sinter. However, some wafers were processed through the entire double metal process and final passivation to evaluate the impact of the entire process on ferroelectric electrical properties.

TABLE 3-8: Process variables for BMF FEMFET device wafers

Wafer Id.	Deposition #	Silicide	Barrier	Thickness	Capping Layer	Top Electrode
7620-6	102	Yes	None	2kÅ	500Å LTO	Ti / Al / TiW
7620-5	103	Yes	None	2kÅ	500Å LTO	Ti / Al / TiW
7620-2	104	Yes	None	2kÅ	500Å LTO	Ti / Al / TiW
7620-3	105	Yes	None	2kÅ	500Å LTO	Ti / Al / TiW
7806-1	131	Yes	None	2.5kÅ	500Å LTO	Ti / Al / TiW
7806-2	132	Yes	None	2.5kÅ	500Å LTO	Ti / Al / TiW
7806-3	133	Yes	None	2.5kÅ	500Å LTO	Ti / Al / TiW
7806-4	134	Yes	None	2.5kÅ	500Å LTO	Ti / Al / TiW
7806-5	135	Yes	None	2.5kÅ	500Å LTO	Ti / Al / TiW
7806-6	143	Yes	None	2.5kÅ	500Å LTO	Ti / Al / TiW
7786-1	147	Yes	None	2.8kÅ	500Å LTO	Ti / Al / TiW
7786-4	148	Yes	None	2.8kÅ	500Å LTO	
7786-5	149	No	None	2.8kÅ	500Å LTO	Ti / Al / TiW
7786-6	170	No	133Å ThrmlOx	3kÅ	500Å LTO	

To electrically characterize the FEMFETs, it was decided that the best approach would be to use conventional log drain current (IDS) versus gate voltage (VGS) I-V curves. By plotting log of drain current, OFF state FEMFET leakage can be seen with picoampere accuracy. The threshold voltage and peak ON current are also easily seen on these plots. FEMFETs were tested by performing a series of DC gate voltage sweeps for $\pm$ 5, $\pm$10, $\pm$20, and $\pm$40 V. Typical sweep rate was approximately 2 Volts per second. Multiple sweeps were generally performed to assess such issues as threshold voltage versus maximum programming voltage, threshold voltage repeatability, and voltage polarity effects. An HP Model 4145B Semiconductor Parameter Analyzer (SPA) for these measurements.

Retention measurements were performed by programming FEMFETs with gate voltages between 10 and 40 Volts for 10 seconds. FEMFETs were then monitored for drain current for 0 volt gate bias (VDS = 1 to 5V). This bias replicates the bias that would be seen in an EEPROM application and allows data to be retrieved nondestructively.

Characterization of the BMF FEMFET devices involved establishing test procedures for these memory transistors. Procedures similar to those used for SONOS nonvolatile memory transistors were used as a starting point. However, it was determined that the ferroelectric films were more prone to deprogramming at low gate biases and extra precautions had to be taken to get valid electrical results. The key lessons learned on BMF FEMFETs were as follows:

1. BMF thicknesses below 2.5 kÅ gave minimal ferroelectric response when first metal was deposited over it.
2. BMF could be successfully grown without a buffer oxide under the BMF with no evidence of SONOS-like charge tunnelling.
3. Most BMF wafers processed had ferroelectric electrical behavior with memory windows typically varying from 1-2 V for 5V programming to 5-20V with 40V programming.
4. Some geometry dependence was observed - "encapsulated" ferroelectric structure tended to have a smaller but more repeatable memory window.
5. Many nonfunctional FEMFETs tended to be stuck in a large negative threshold voltage state, indicating positive ferroelectric polarization at the silicon-FE interface
6. BMF films evaluated had typical memory retention times on the order of 1 to 5 hours.
7. Source follower configuration retention measurements indicated this approach gave no improvement in FEMFET retention.

Initial BMF FEMFET device wafers showed no ferroelectric response despite very positive results from gridded CV wafers. Further investigation of this issue indicated that the gridded test wafers used a thinner metallization layer than that used for the FEMFET device wafers. It was postulated that stress related effects were causing this loss in ferroelectric response. Gridded CV wafers were then fabricated which confirmed this theory. Increasing the BMF film to 2.5 kÅ was shown to give ferroelectric electrical characteristics on both gridded and device wafers with the baseline first metal process.

Some examples of BMF FEMFET I-V characteristics from one of the first device wafers is shown in Figure 3-30. Note that when gate voltage is ramped from positive to negative voltage, the transistor threshold tends to be pushed negatively (toward depletion mode operation). Conversely, ramping gate voltage from negative to positive voltage shifts transistor thresholds positively (towards enhancement mode operation). These shifts are opposite in direction to what is seen for SONOS memory devices which rely on charge trapping for memory operation. The opposite nature of these shifts confirmed that ferroelectric operation was being observed in these BMF FEMFETs.

One observation from initial BMF FEMFET device wafers was that encapsulating the ferroelectric with metallization tended to give a smaller ferroelectric memory window than what was being seen on gridded CV wafers. This was also seen when measuring FEMFETs designed to minimize encapsulation by metallization. Figures 3-31 and 3-32 show that an encapsulated FEMFET from 7806-3 and 7806-4 had about a 2-6V memory window with 20V programming, compared to a 10V window for a FEMFET without

encapsulation. It was presumed that this was a stress related effect. Since EEPROM sense amplifier circuitry can detect memory windows as low as 100 mV, it was decided that this memory window size would be adequate for demonstration of a FERRAM memory.

To further evaluate stress related issues and the impact of double metal processing on FEMFET characteristics, device wafers were processed through the Westinghouse double metal process with final overcoat passivation and sinter. Figures 3-33 and 3-34 show typical characteristics from encapsulated and unencapsulated FEMFETs. While some degradation in memory window size was observed after overcoat, in general, this degradation was minimal. Typical memory window sizes for 20V programming were 2V for encapsulated FEMFETs and 8-12V for unencapsulated FEMFETs. From a reliability and manufacturability standpoint, it was decided that the preferred FEMFET approach would be the encapsulated design approach. This approach was employed in the 8K FERRAM, and it was decided to focus all subsequent FEMFET characterization on these encapsulated FEMFETs.

Initial attempts to measure BMF FEMFET retention indicated retention times of under 10 minutes. However, this initial problem was traced to a test set-up problem. It was determined that the original test set-up used unshielded cabling, and it was suspected that electrical noise was interfering with the BMF FEMFET retention measurements. This problem was resolved by transferring to a test stand with coaxially shielded cables.

To verify validity of the FEMFET retention measurements, Westinghouse SONOS transistors were measured using the proposed FEMFET retention tests. Figure 3-35 shows the resulting SONOS drain current retention data. For retention the drain current with 0V gate bias and 5V drain bias was monitored versus time. Note that excellent retention was observed, with minimal change in drain current after 4000 seconds. Also note that this memory device had a 4V memory window with a 10V program voltage. These measurements confirmed that these retention measurement techniques were valid for memory transistors.

A series of measurements were then performed to quantify the retention characteristics of the BMF FEMFETs. In general, all of these evaluations indicated that the BMF FEMFETs that were fabricated had retention, with typical times of 1 to 5 hours. These results are summarized in Figures 3-36 through 3-40. These figures show various techniques which were evaluated in an effort to improve retention results. These techniques included source-follower transistor configuration, strobing of FEMFET drain current, and alternate gate biasing. None of these approaches gave improvements in retention.

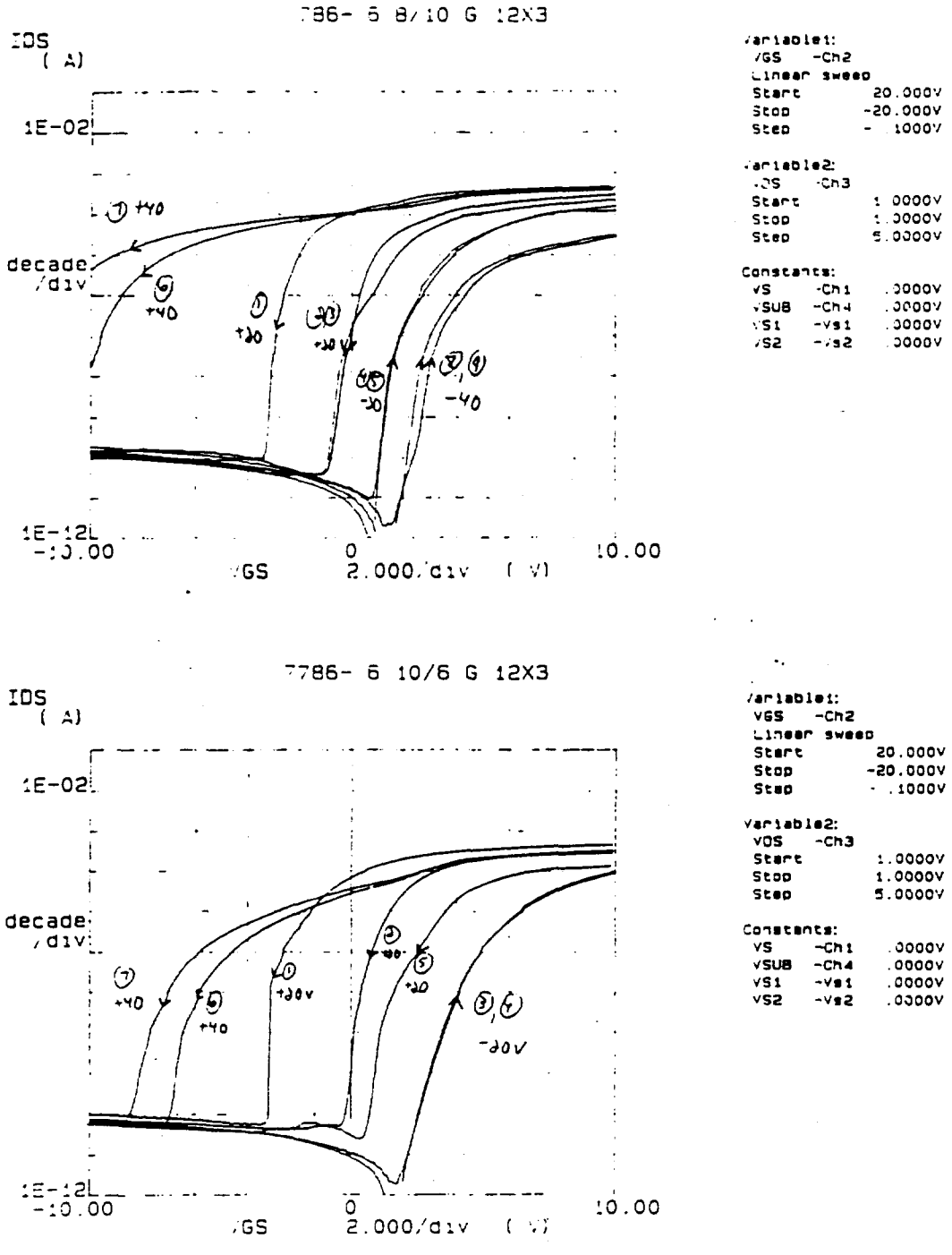


Figure 3-30: Initial BMF FEMFETs Demonstrated Ferroelectric Behavior.

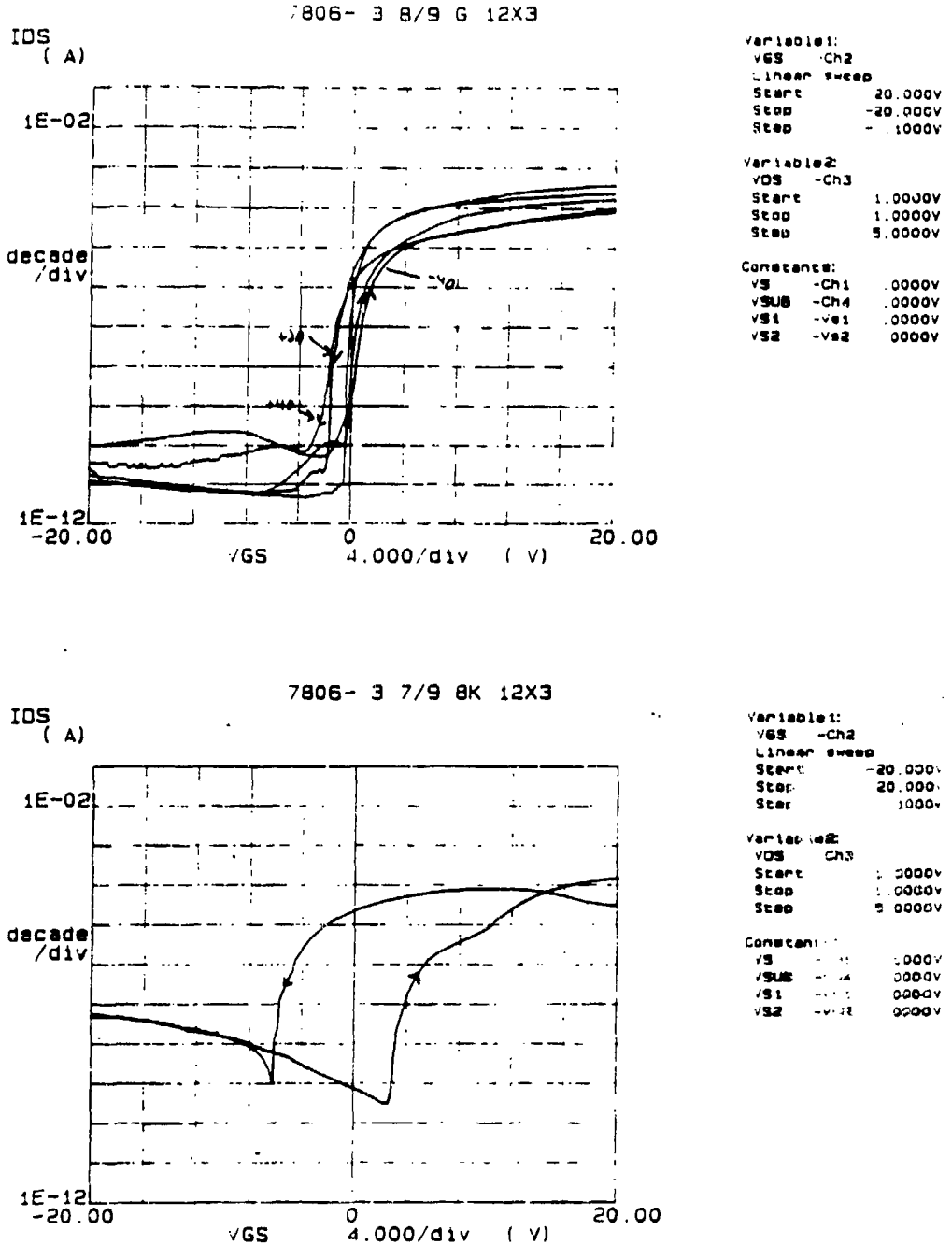


Figure 3-31: Metal Encapsulation of Ferroelectric Reduced BMF FEMFET Memory Window Size From 10V (Bottom) to 2V (Top) With 20V Programming

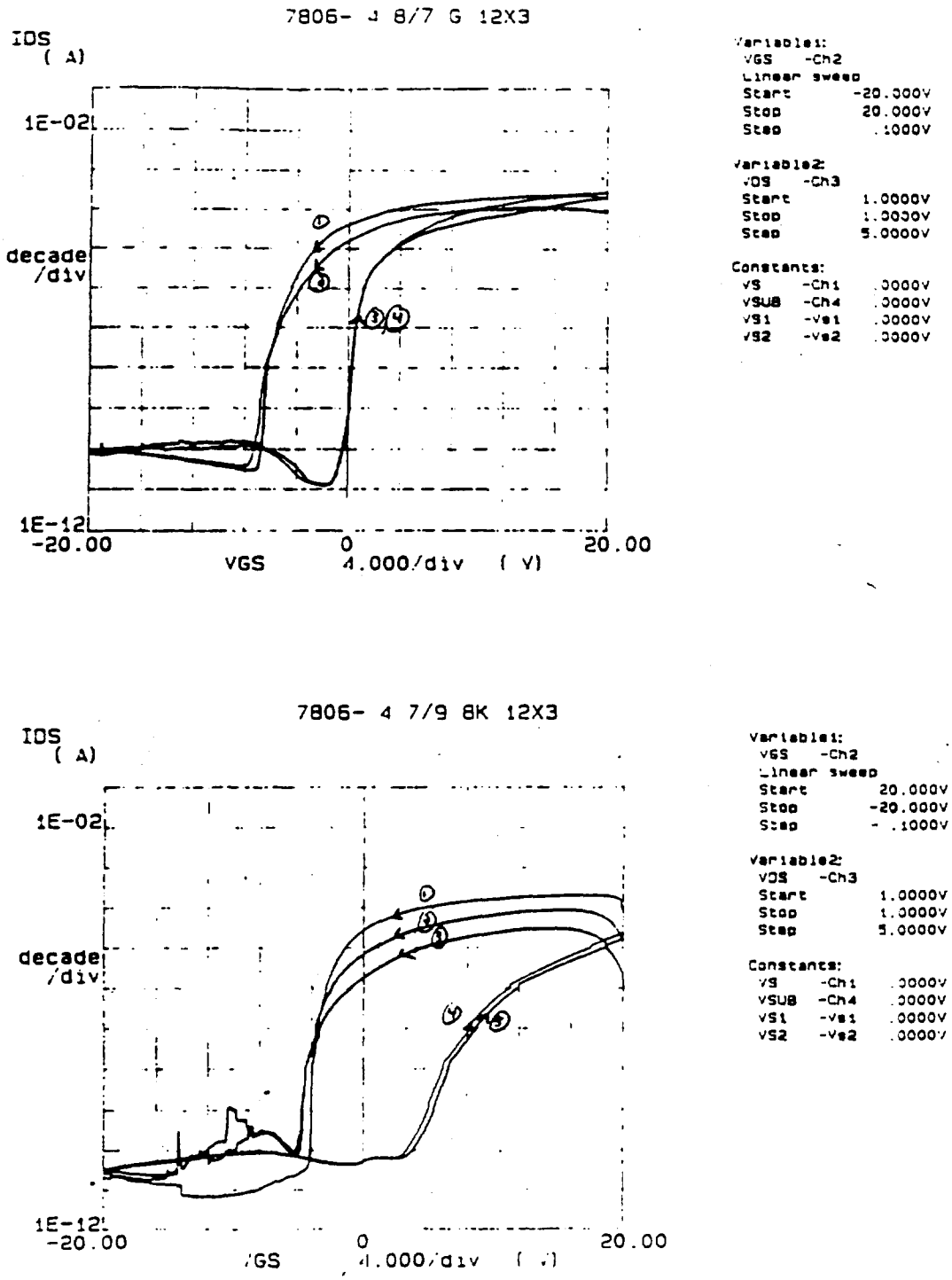


Figure 3-32: Metal Encapsulation of Ferroelectric Reduces BMF FEMFET Memory Window Size From 10V (Bottom) to 6V (Top) With 20V Programming.

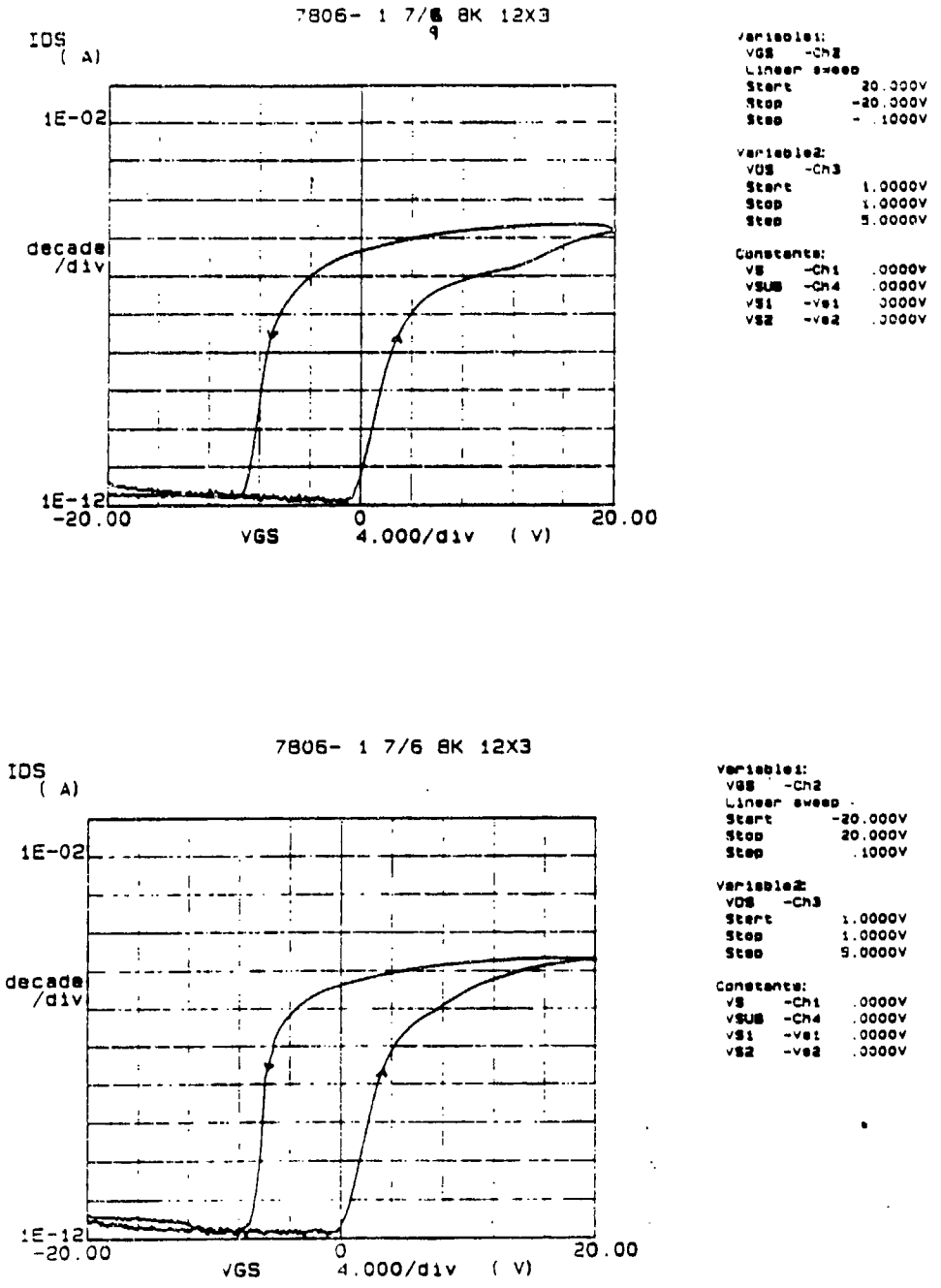


Figure 3-33: After Final Overcoat and Sinter Processes, Unencapsulated BMF FEMFET Has 8-12V Memory Window With 20V Programming

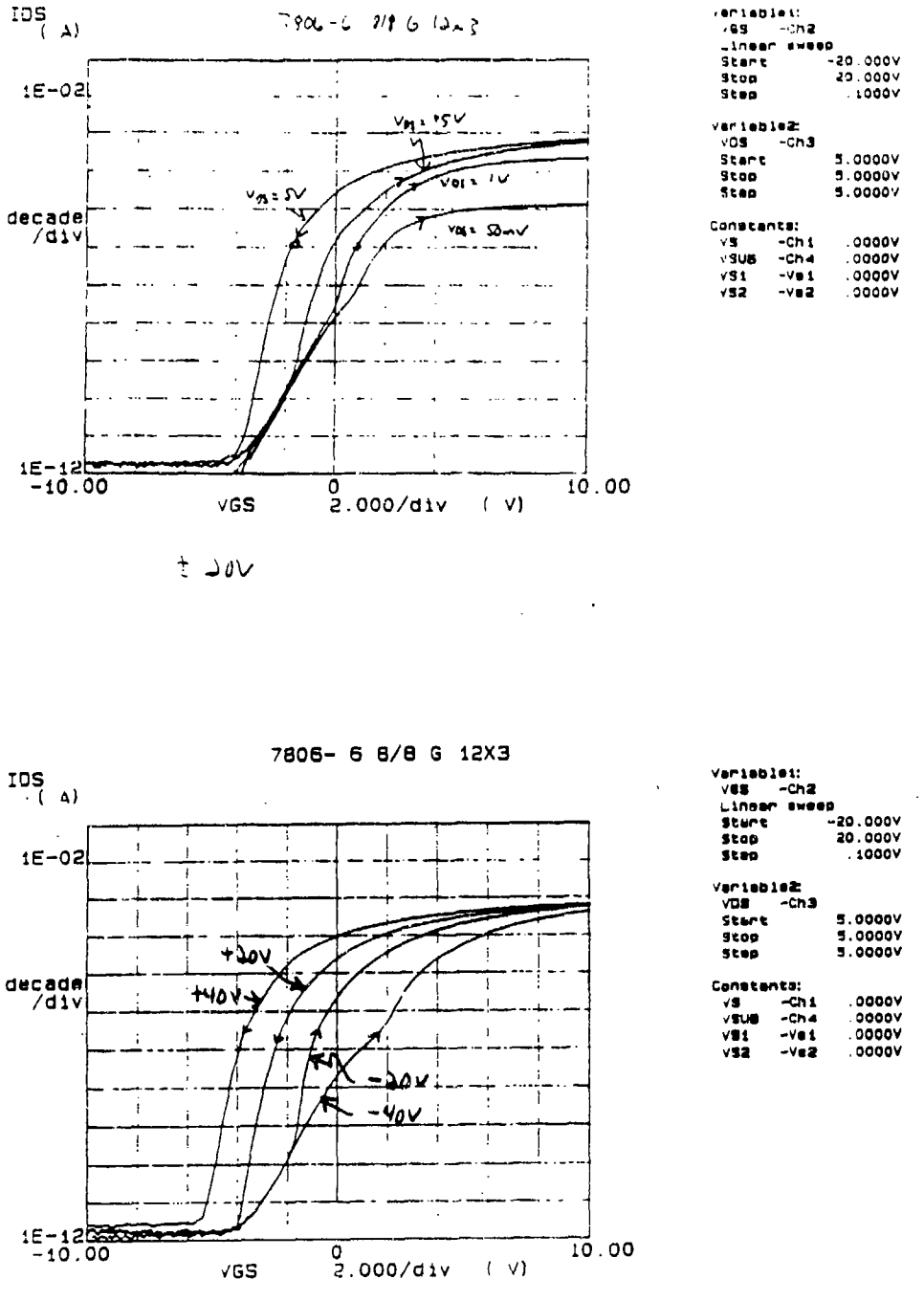
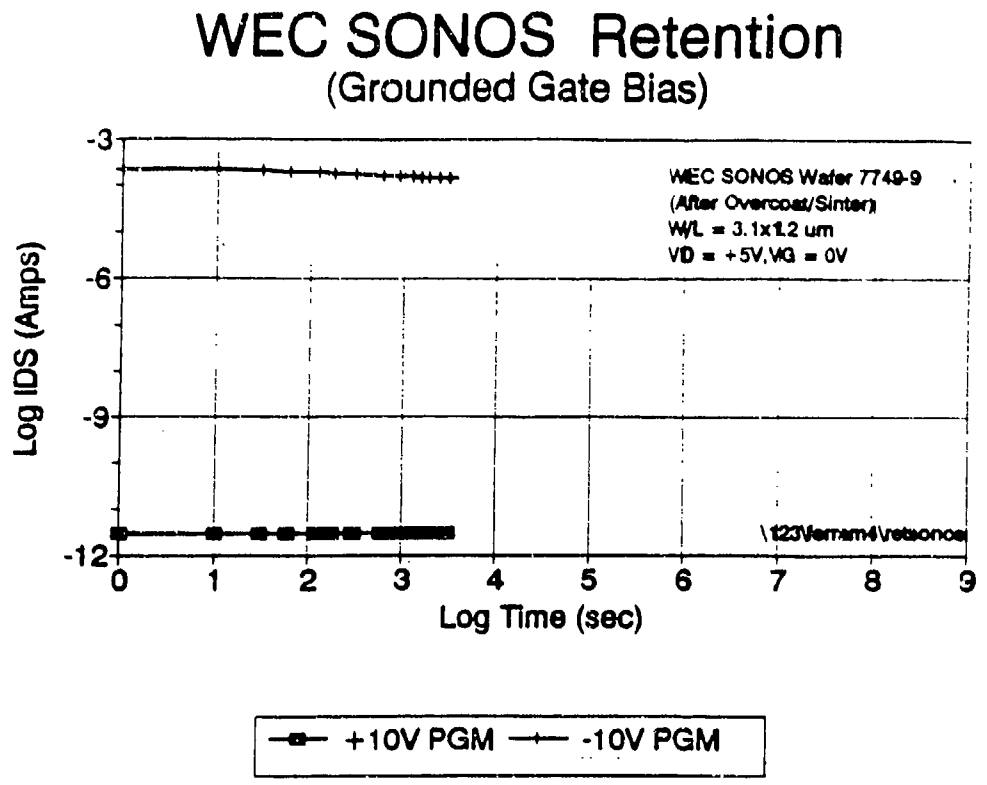


Figure 3-34: After Final Overcoat and Sinter Processes, Encapsulated BMF FEMFET Has 1-2V Memory Window With 20V Programming



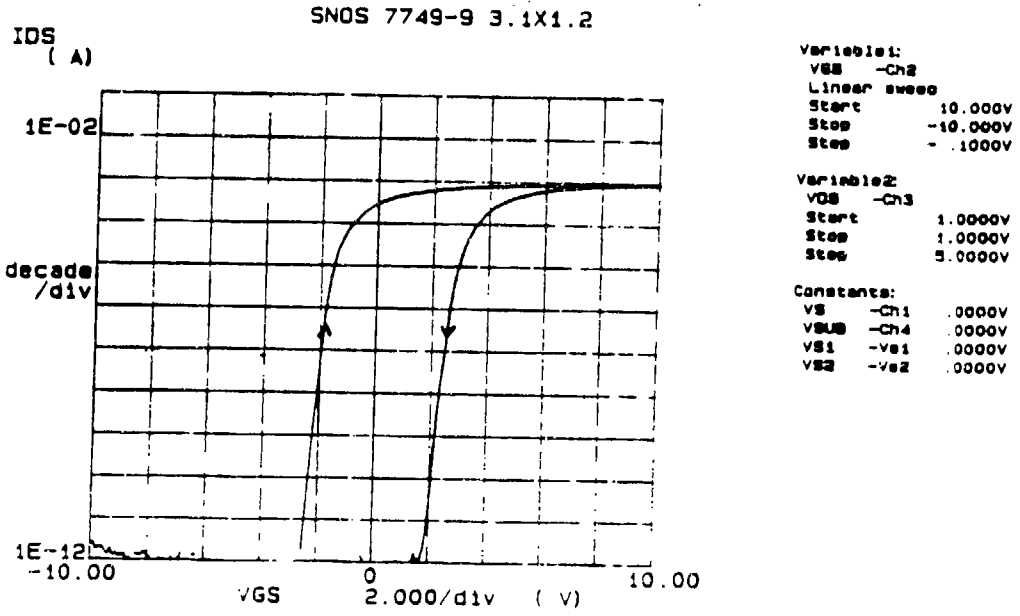


Figure 3-35: Westinghouse SONOS Transistors Show Excellent Retention to Validate FEMFET Retention Measurement Techniques.

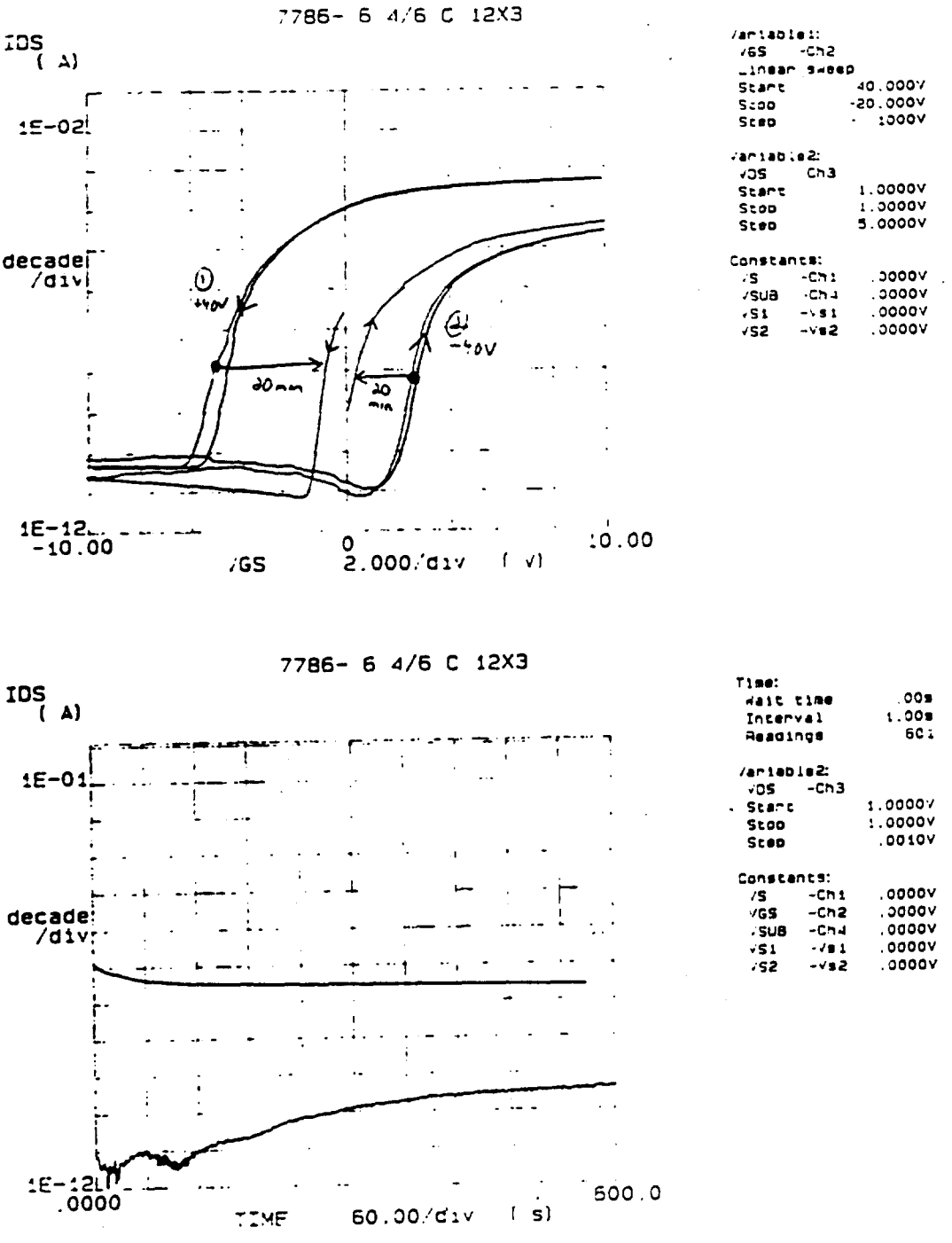


Figure 3-36: BMF FEMFETs Indicate Less Than 1 Hour Retention With Standard Grounded Gate Configuration.

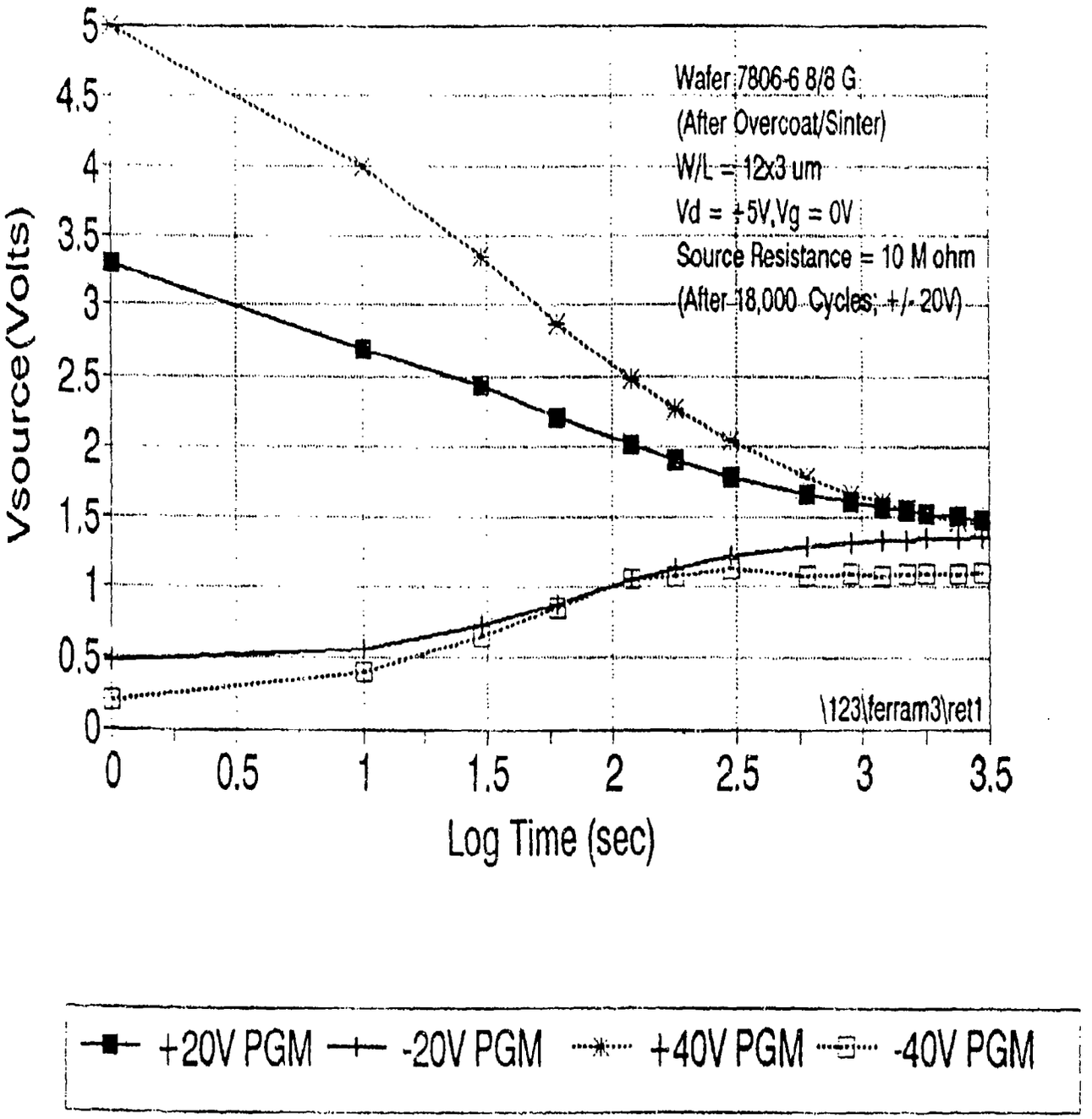
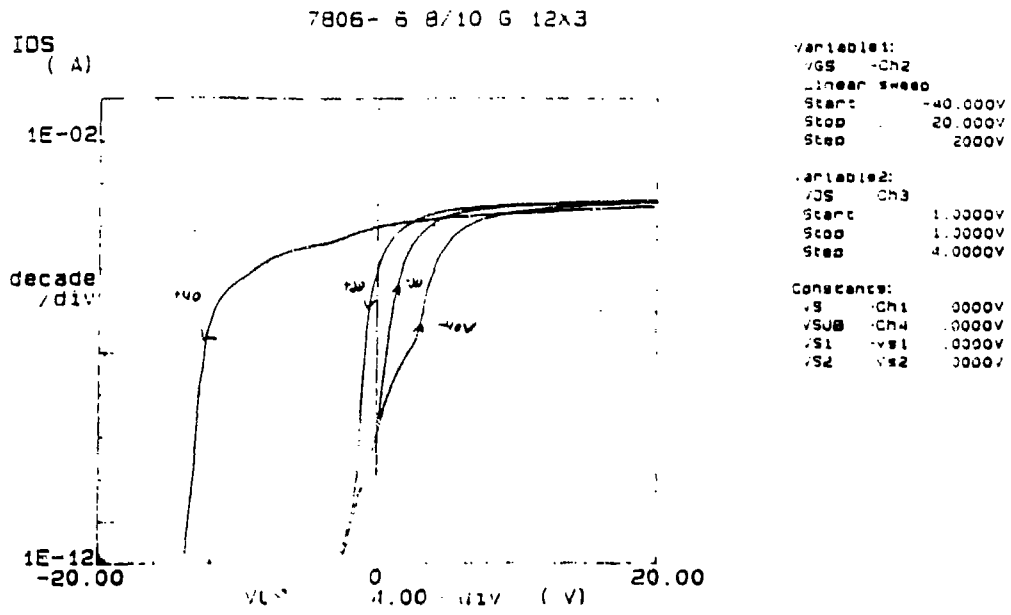


Figure 3-37: BMF FEMFET Retention Unimproved By Source-follower Configuration.



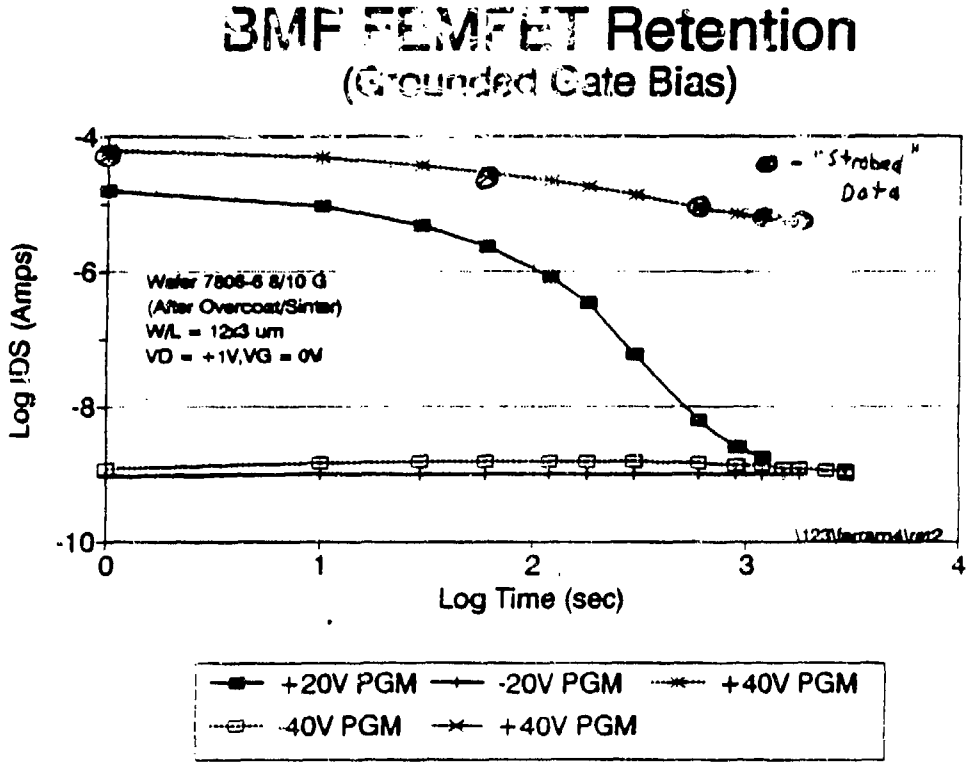
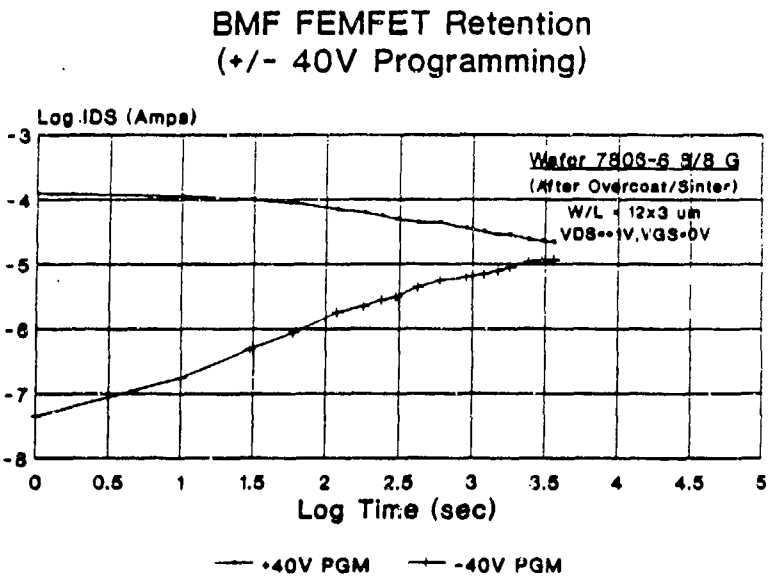


Figure 3-38: BMF FEMFET Retention Unimproved By Strobing Drain Current.



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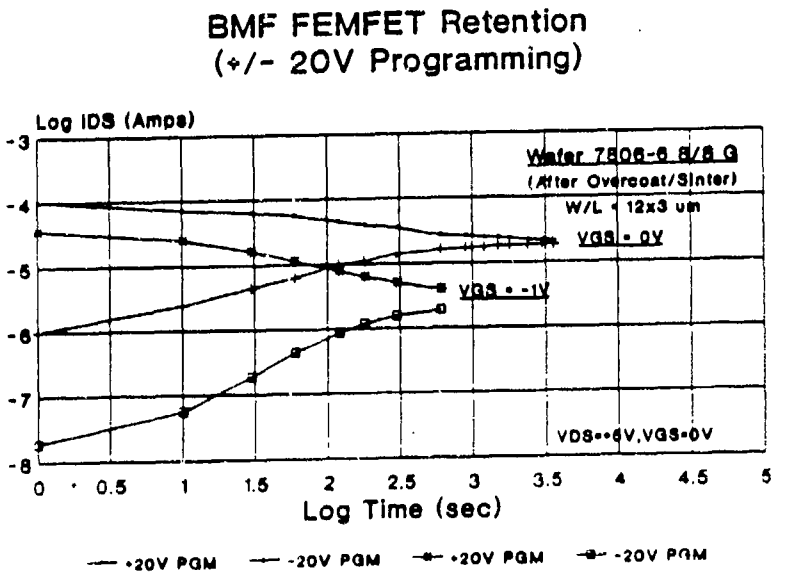
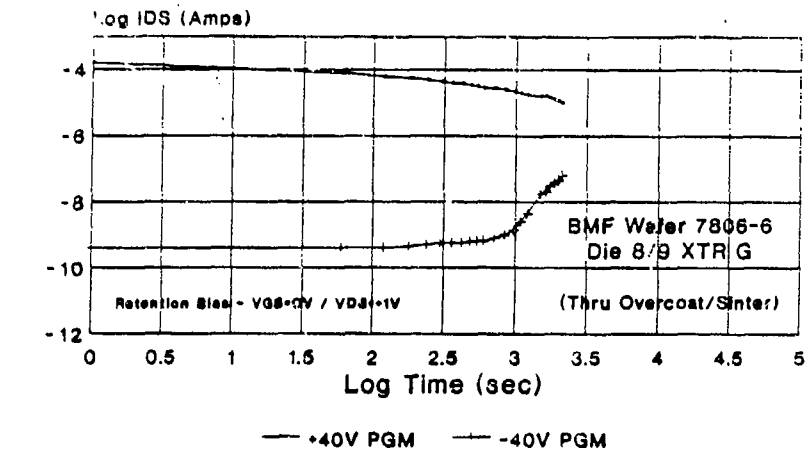


Figure 3-39: BMF FEMFET Retention Unimproved By Alternate Gate Bias.



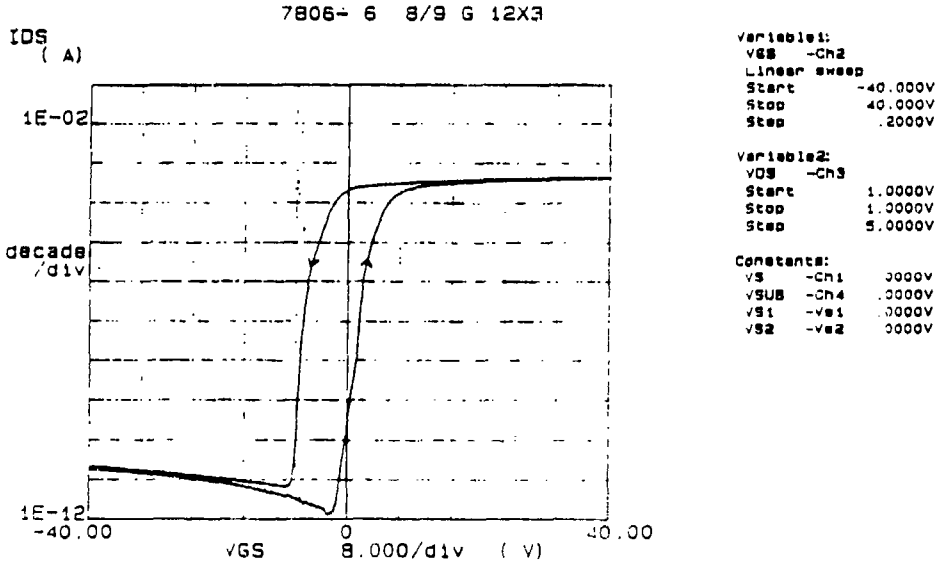


Figure 3-40: Typical BMF FEMFET Retention Measurements (Indicate Between 1 and 5 Hours)

3.7.1 Thickness Effect on the Memory Window

Capacitance - Voltage (CV) measurements of memory windows showed that a difference existed on window size between mercury probe and aluminum capacitor dot measurements on the same wafer. Also that the ratio of (mercury probe window to aluminum dot window) varied with the thickness of the BMF film between different wafers. This effect was initially noted on a gridded test wafer which has a 10nm buffer thermal oxide - 100nm BMF layer - 50nm low temperature oxide (LTO) Cap. Mercury probe C-V measurements showed a memory window of several volts for a $\pm$10V sweep. Then after aluminum dots were evaporated through a shadow mask on top of the capping layer the C-V measurement showed that the memory window was gone. Another wafer sample with a BMF thickness of 200nm was C-V evaluated. This time a reduced but measurable aluminum dot memory window was observed compared to the mercury probe value. These results point to the fact that all ferroelectric materials are also piezoelectric. Therefore a strain induced in a ferroelectric thin film will translate into an electrical effect. For sufficiently thin layers of BMF, i.e. 100 nm, the strain produced by the aluminum dot was sufficient to suppress the memory window. As the ferroelectric layer was increased in thickness, the interfacial strain was relaxed in the internal volume and the ferroelectric memory window was restored to varying degrees depending on the thickness of the BMF thin film. To quantify memory window size to thickness of BMF, the ratio of mercury probe window to aluminum dot window was plotted for a number of BMF wafer samples with different ferroelectric thickness as shown in Figure 3-41. This data indicated that a minimum BMF thickness of about 283nm was required to obtain a memory window that was minimally reduced in magnitude for an aluminum dot compared to a mercury probe which does not apply mechanical stress to the structure.

Subsequently to the above study of BMF thickness/memory window relationship, a paper [17] appeared in "Physical Review Letters", which reported on strain relaxation by domain formation in epitaxial ferroelectric thin films. This paper showed that for film thickness greater than 250nm the interfacial strain is relieved. These results appear to agree and support our limited test results discussed above.

The induced strain effect on the memory window clearly indicates that it is a factor that needs to be considered in the design of nonvolatile memory transistors. Thickness of the ferroelectric film, structure geometry and fabrication process that minimize the strain in the thin memory film all need to be addressed. Choice of a material that would provide good ferroelectric properties and at the same time have a minimal piezoelectric response may be another option.

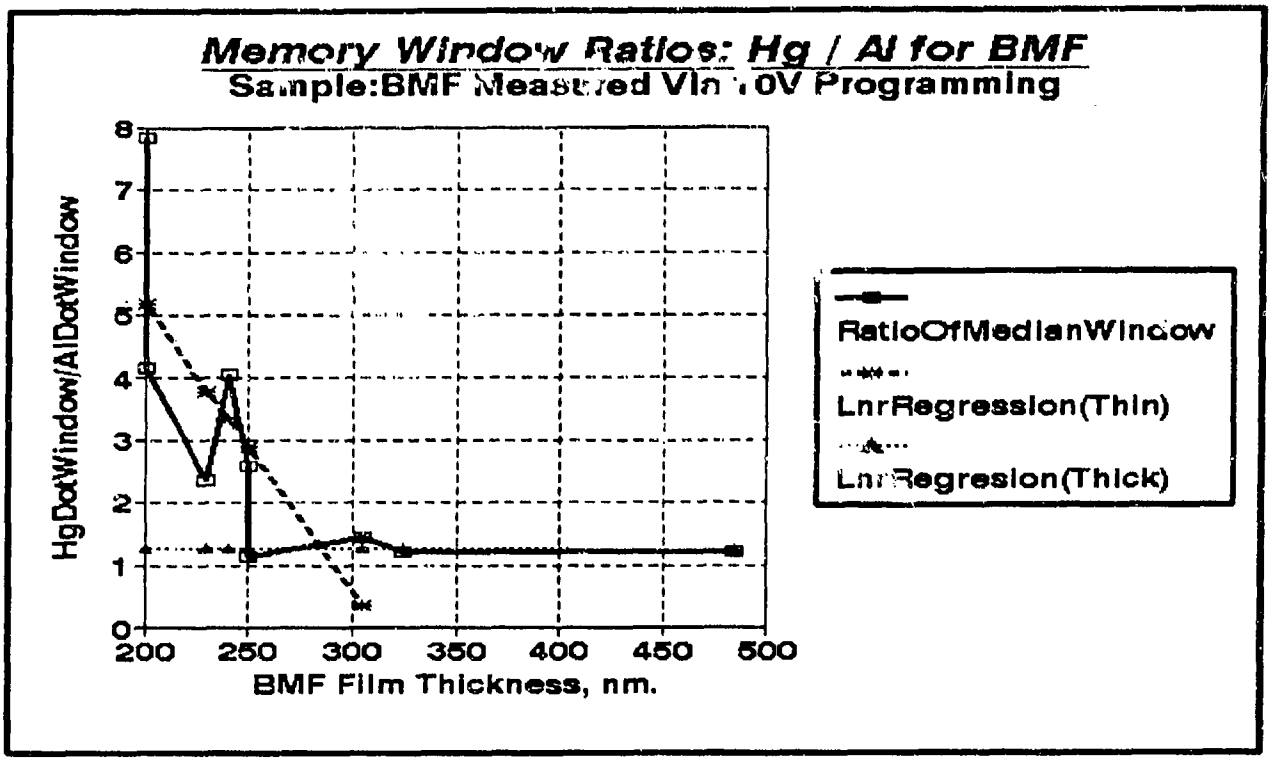


Figure 3-41: Ratio of Mercury Probe Memory Window to Al Dot Memory Window vs BMF Thickness

.4.0 DISCUSSION OF BMF RESULTS AND CONCLUSIONS

The primary objective of this portion of the program was to develop a high-performance ferroelectric BMF gate dielectric for a FEMFET-FERRAM array, which would offer large memory-window characteristics under low address voltage conditions, with good storage stability. The first two criteria have essentially been met, using BMF films grown at low temperatures on silicon and annealed at elevated temperatures to promote crystallization of the ferroelectric phase. However, although film structures capable of displaying relatively large switched polarization were produced, memory performance fell significantly short of the expected goals because of poor retention characteristics.

High vacuum deposition parameters were established that provided good quality BMF films that showed memory windows as large or larger than the write voltage. Stress effects on the ferroelectric properties of BMF films were suggested for ultra-thin BMF films, with a minimum thickness of about 200 nm needed to retain ferroelectric response. A number of test transistors were fabricated with a BMF gate dielectric that showed good transistor curves; however, the retention time was on the order of one to five hours. Further retention and temperature-bias- stress evaluations indicated that mobile charges were a significant factor in producing a fast decay rate of the memory window. On the other hand the measurements on BMF films using the RT-66A test system showed that the ferroelectric spontaneous polarization, Ps, diminished only slightly under endurance cycling.

Ionic conductivity is also a problem with BMF as operating temperature is increased above 25°C. Group II fluorides (MgF_2, CaF_2, SrF_2, and BaF_2) are known to be ionic conductors, exhibiting conductive behavior at higher temperatures. The only information available on the ionic conductivity of BMF is that

published by DiDomenico et al[7], who stated that $BaMF_4$ single crystals exhibit a low frequency (1 kHz) conductivity along a, b, and c axes which increases approximately exponentially on heating toward the melting point. Numerical data were not provided for BMF in reference 7. Fielder[8], who performed detailed measurements of ionic conductivity in solid barium fluoride single crystals, observed conductive behavior from about 160°C to 890°C in that material. Three regions were identified: 1) extrinsic, 2) lower intrinsic, and 3) upper intrinsic. In the extrinsic region (impurity controlled) the specific conductivity, K_S could be expressed as,

$$K_S = 1.3\exp(-23000/RT) \text{ ohm}^{-1}\text{cm}^{-1}$$

where R is the gas constant (calories/degree) and T is the absolute temperature. The rate equations for the lower and upper intrinsic regions respectively were given by,

$$K_S = 3.78X10^4 \exp(-32700/RT) \text{ ohm}^{-1}\text{cm}^{-1} \text{ , and}$$

$$K_S = 2.05X10^5 \exp(-35600/RT) \text{ ohm}^{-1}\text{cm}^{-1} \text{ .}$$

The thermally produced defects, responsible for the conductivity of solid barium fluoride in the intrinsic region, were suggested to be fluorine ion vacancies and fluorine ions in interstitial sites. The defects could be produced by impurities in the extrinsic region. Assuming that BMF follows a similar conductive behavior, the ionic conductivity should be negligible at room temperature, and should depend on impurity content and defect density at higher temperatures. It is essential that the starting materials in the synthesis of the BMF film be of high purity. Ideally the thin film should also be single crystalline, free of any defects.

Our experimental results and analysis have shown that a significant contributor to the leakage of the uncapped BMF film is film cracking (caused by differential thermal expansion), and associated intergranular penetration of the gate electrode. This was alleviated by application of a high quality SiO_2 capping layer, but resulted in the need for higher programming voltages. Earlier results on films vacuum-annealed at 600°C, in addition to very recent measurements on films crystallized by the RTA method at temperatures in the range 550°C to 700°C, have revealed that higher annealing temperatures produce a significant lowering of the coercive field. Similar results have been reported recently by Shi et al.[16] for PZT films. A preliminary result for an uncapped film (see Figure 3-42) has shown that RTA at 650°C can result in remanent switched polarization values of about 0.4 $\mu C/cm^2$ using applied voltage amplitudes of 5 V (i.e. field strengths of about 200 kV/cm).

Studies reported here also have demonstrated the large magnitude of elastic tensile stress developed in BMF films grown on silicon substrates. These stresses in turn generate piezoelectrically induced electric fields within the film, which may account for our observation of clamped negative thresholds in non-functioning FEMFET devices, and hence the occurrence of residual positive polarization near the FE/Si interface. Superimposed on this picture also are intrinsic and/or thermal stresses induced in the ferroelectric layer by deposition of electrode layers such as Al as well as other overlying layers. We tentatively attribute the observed poor retention in BMF and some other ferroelectric gate dielectrics to the drift of mobile charge, which may be aggravated by the existence of stress-induced internal fields. It should be feasible (along the lines we have sucessfully explored for bismuth titanate and related gate dielectrics), to significantly suppress the mobile-ion effects in BMF layers, by employing chemical doping approaches. Candidate "dopants" might include Sr or La substituting for Ba; Ta substituting for Mg; or O substituting for F. In particular, site substitutions between O and F are well-known, and numerous ferroelectric oxyfluorides have been studied[18].

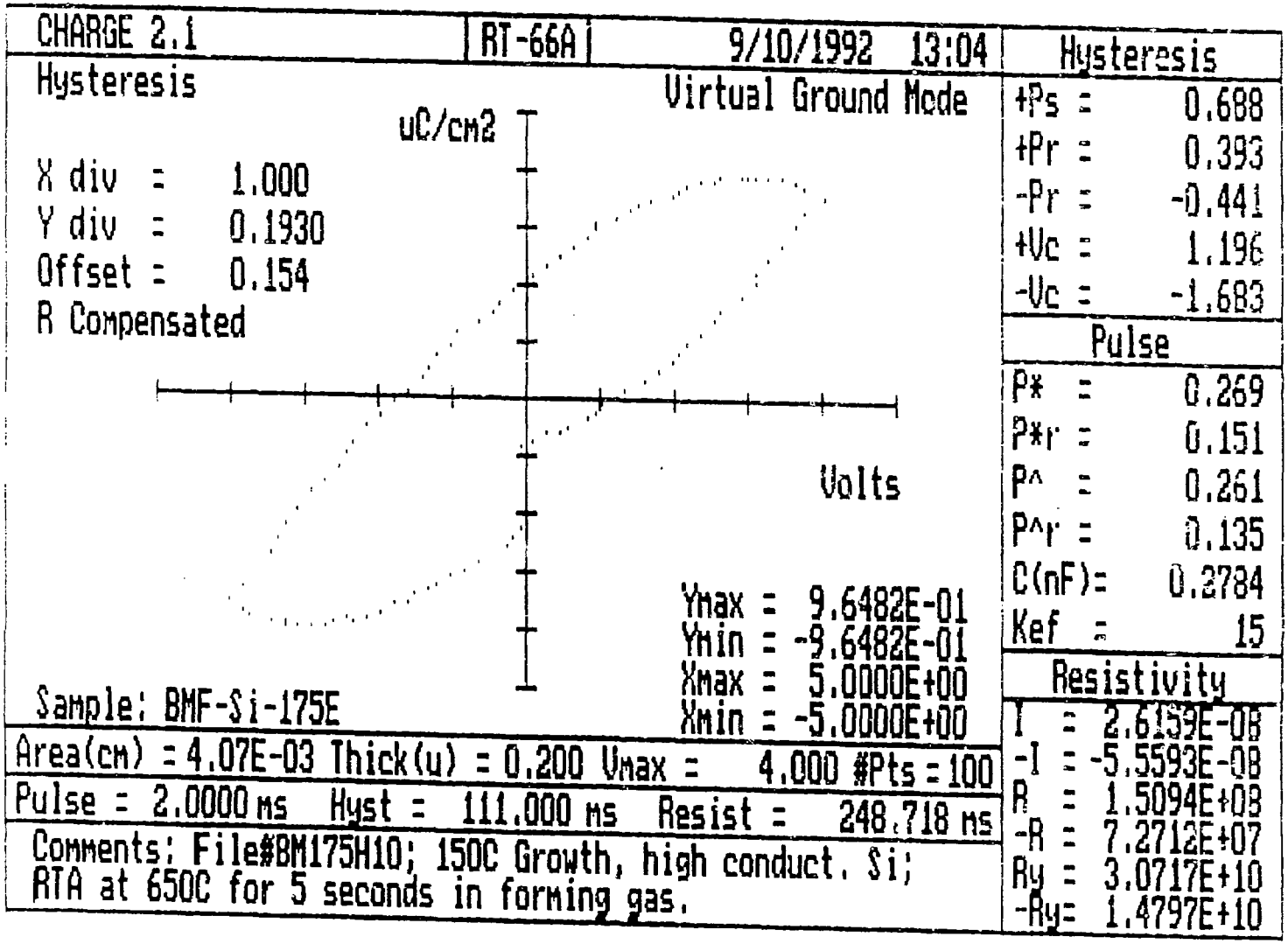


Figure 3-42: BMF Film RTA Annealed At 650°C

5.0 RECOMMENDATIONS

The relatively short retention times of several hours coupled with ionic conductivity at higher temperatures indicates that the choice of BMF as the ferroelectric gate material in a non-volatile FET be shifted to other materials. Review of the literature suggests that bismuth titanate or other oxide-based ferroelectric material, appropriately doped and optimally processed, is a good candidate.

Furthermore, we believe that the use and optimization of RTA crystallization approaches, will (as has been proven for PZT layers) result in FE film products of much enhanced electrical integrity, and in the reduction of the threshhold drift or leakage effects. This should in turn reduce the need for capping layers. The marked reduction in coercive fields, resulting from the possible use of higher RTA processing temperatures, will also allow us to move towards significantly lower programming voltages; this is clearly an important consideration in the operation of large, high-speed memory arrays.

6.0 REFERENCES

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Appendix A: Tables Summarizing BMF Wafer History

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C), Duration	Monitor Thickns, Rate (nm), (Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Film Co
BMF-Si-1	p-/p++		950, 10Min.	1100-1250	550, 75 Min.	307, 0.8-1.2	Thick, flaking		Not used			BMF-Si-1
BMF-Si-2	Grided SA-NO8		950, 10 Min.	1175-1195	550, 60 Min.	60, 0.2-0.3	600-340		Warped wafer, to ATL			BMF-2
BMF-Si-3	Grided SA-PO7		950, 10 Min.	1185	550, 52 Min.	50, 0.1-0.2	680-480		Ellipsometry, to ATL			BMF-3
BMF-Si-4	Grided SA-PO6		900, 10 Min.	1175	550, 21 Min.	15, 0.1-0.2	300-1500		To ATL			BMF-Si-4
BMF-Si-5	.005-.02, N		900, 10 Min.	1100,new mat	550, 38 Min.	40, 0.1-0.2	600-500		X-ray, hysteresis	Multi-epi with <011> up and <001> almost up + poly BaF_2		BMF-5
BMF-Si-6	p-/p++		900, 10 Min.	1100	550, 9 Min.	10, 0.1-0.3	200-100		To ATL			BMF-Si-6
BMF-Si-7	p-/p++		900, 10 Min.	1100	550, 11 Min.	12.5, 0.2-0.4	200-100		To ATL			BMF-Si-7
BMF-Si-8	Grided FM-N01		700, 10 Min.	1100	550, 9 Min.	10, 0.2-0.3	250-150		To ATL			BMF-8
BMF-Si-9	Grided FM-N02		800, 10 Min.	1100	550, 10 Min.	10, 0.1-0.3	310-150		To ATL			BMF-Si-9
BMF-Si-10	.005-.02 Ω-cm, N-type		800, 10 Min.	1100	550, 17 Min.	15.8, 0.1-0.3	530-330		X-ray, RTA, SiO_2,	Multi-epi + Some BaF_2 with <111> fiber texture.	Hysteresis, to PSU	BMF-10
BMF-Si-11	Grided FM-N04		800, 10 Min.	1100	550, 12 Min.	12, 0.1-0.2	310-150		700°C RTA 20sec in Forming Gas, to ATL			BMF-11
BMF-Si-12	Grided FM-N05		800, 10 Min.	1100	400, 11 Min.	10, 0.1-0.2	250-150		To ATL			BMF-Si-12
BMF-Si-13	.005-.02, N		900, 10 Min.	1085,new mat	350, 11.5Min	15, 0.1-0.3	310-150		Anneal for 30 min. in vacuum furnace at 600°C.	X-ray: Amorphous as grown; Poly with <010> fiber textr after 600°C	One piece to PSU; Poly, good hysteresi	BMF-13
BMF-Si-14	30-40, N		900, 10 Min.	1085, 1100	550, 56 Min.	100, 0.2-0.4	~2μm		Flaking, not used, Krish			BMF-14
BMF-Si-15	1μ pt/50nm SiO_2/.005-.02 Ω-cm,N		500	1085	500, 23.5Min	30, 0.1-0.3	650-500		Flaking, not used			BMF-Si-15
BMF-Si-16	Patterned, ATL #19511-15		700, 10 Min.	1085	500, 6'13"	8, 0.2-0.3	160-100		To ATL			BMF-Si-16
BMF-Si-17	Patterned, ATL #19511-14		700, 10 Min.	1085	500, 7'39"	8, 0.1-0.3	160-100		To ATL			BMF-17
BMF-Si-18	Patterned, ATL #19511-16		700, 10 Min.	1085	500, 7'53"	8, 0.1-0.3	160-100		To ATL			BMF-Si-18
BMF-Si-19	30-400-cm N		900, 10 Min.	1100	550, 24'38"	40, 0.2-0.4	850-700		Flaking, not used, Krish			BMF-19
BMF-Si-20	175Å SiO_2 on .005-.02 N		700, 10 Min.	1100	500, 14 Min. 30 Min post- anneal at 550°C	25, 0.3-0.4	500-300		No loop with Cr-Au dots. Good ,D values. Resistive loop with Hg			BMF-20
BMF-Si-21	.005-.02 Ω-cm, N		900, 10 Min.	1075	250, 10 Min., 30 Min. post-anneal at 600°C	8, 0.1-0.2	250-125		Poor hysteresis. vac- anneal 600°C, 30min. Better loop.	Poly+multi- epi after in situ anneal at 600°C for 30 Min. Poly + <010> fiber tex after vac-furnace anneal at 600°C for 30 minutes.	R ≈ 1E50 on RT-66. Too leaky for measurement.	BMF-21
BMF-Si-22	Recycled wafer #19511-14 from ATL		Last HF-etch reduced to 15s. 700, 10 Min.	1075,new mat.	350, 10 Min.	10, 0.1-0.2	250-125		Vac. anneal at 600°C for 30 Min., to ATL.			BMF-Si-22
BMF-Si-23	Recycled wafer #19511-15 from ATL		Same as 22	1085	350, 13 Min.	10, 0.1-0.2	250-125		Same as 22			BMF-Si-23

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C),Duration	Monitor Thckns,Rate (nm),(Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Film Code
BMF-Si-24	p/p+		900, 10 Min.	1075	350, 12 Min.	10, 0.1-0.2	250-125		Vac. anneal at 600°C for 30 Min. To ATL			BMF-Si-24
BMF-Si-25	p/p+		900, 12 Min.	1085	350, 12 Min.	10, 0.1-0.2	250-125		Same anneal as 24, To ATL			BMF-Si-25
BMF-Si-26	p/p+		900, 10 Min.	1085	350, 9 Min.	10, 0.1-0.2	250-125		Same anneal, to ATL			BMF-Si-26
BMF-Si-27	p/p+		900, 10 Min.	1085	350, 10 Min.	10, 0.1-0.2	250-125		Same anneal, to ATL			BMF-Si-27
BMF-Si-28	p/p+		900, 10 Min.	1085	350, 10 Min.	10, 0.1-0.2	250-125		Same anneal, to ATL			BMF-Si-28
BMF-Si-29	p/p++		900, 10 Min	1085	350, 11 Min.	10, 0.1-0.2	300-190 Ellipsometry.		amorphous. Vac-anneal 600°C for 30m, Orient.	Poly+ multi-epi after vac-anneal at 600°C for 30 Min. However, too leaky for RT-66. R=9E50.	H_2 anneal at 500°C, 1 hr., good loop, fatigue test on RT-66 600°C & 700°C in H_2 gradually worse.	BMF-Si-29
BMF-Si-30	p/p++		900, 10 Min.	1085	350, 7 Min.	10, 0.1-0.3	250-125		No anneal, to ATL			BMF-Si-30
BMF-Si-31	p/p++		900, 10 Min.	1075	350, 11 Min.	10, 0.1-0.2	300-180		No anneal, to ATL			BMF-Si-31
BMF-Si-32	p/p++		900, 10 Min.	1075	550, 13 Min.	10, 0.1-0.2	310-190		No anneal, to ATL			BMF-Si-32
BMF-Si-33	660nmTi-Pt/ 50nmSiO_2/n, .005-.020-cm		900, 10 Min.	1075	500, 22 Min.	15, 0.1-0.2	520-320 (DEKTAK)		X-ray, poly, some100 poor adhesion, Al back hysteresis, breakdown.	Poly with some preferred <100>		BMF-Si-33
BMF-Si-34	.005-.020-cm, n-type		900, 10 Min.	1085	450, 15 Min.	10, 0.1 0.2	300-180		X-ray, oriented poly.	Multiple epitaxial structure as before.		BMF-Si-34
BMF-Si-35	.005-.020-cm, n-type		900, 10 Min.	1085	400, 10 Min.	10, 0.2	250-125		X-ray, oriented poly. H_2 anneal, X-ray.	Multiple epitaxial structure as before.		BMF-Si-35
BMF-Si-36	.005-.020-cm, n-type		900, 10 Min.	1085	300,12 Min.	10, 0.1-0.2	250-125		X-ray, amorphous. H_2 anneal at 400,500 600,700°C for 1hr.	Amorphous as grown. 1hr H_2 anneal at four diff. temps. Amorphous at 400°C, poly with some <011> orientation at 500 Poly with some <100> fib. tex. BaF_2 at 600°C, and only BaF_2 with <100> fiber texture after 700°C anneal.	X-ray, hysteresis.	BMF-Si-36
BMF-Si-37	570nm Ni/50 nm Ti/50nm SiO_2/p/p++Si		None	1075, New Mat.	500, 11 Min.	15, 0.1-0.3	350-218 DEKTAK at edge		Patchy film, good adhesion, Al-backcoat one quadrant, poor hysteresis. X-ray, varying.	Poly $BaMgF_4$ + unidentified phase (No Ni) a center. Only <111> fiber textured Ni at masked outer edge. Ni gradually replaced by $BaMgF_4$ + unidentified phase as we move toward center.		BMF-Si-37
BMF-Si-38	Grided FM-N07		900, 10 Min.	1075	350, 10 Min.	10, 0.1-0.3	200-125		to ATL			BMF-Si-38
BMF-Si-39	Grided FM-N08		900, 10 Min.	1075	350, 9 Min.	10, 0.1-0.3	250-125		to ATL			BMF-Si-39
BMF-Si-40	36.4nm a-Si/ .002-.050-cm		350	1075	350, 8 Min.	10, 0.1-0.3	250-125		Vac-anneal 550°C for 30 min.	Amorphous as grown, preferred <010> fiber texture after vacuum anneal.	R=1E50 and R_H=2E70-cm on RT-66. Too leaky for measurement.	BMF-Si-40
BMF-Si-41	288nmAl/40nm SiO_2/4-80-cm N/N++		450	1075	450, 11.5 Min.	15, 0.1-0.3	212.7nm at edge by DEKTAK		504nm Al back-coat on one half. Unopened hysteresis, low volts.	Highly polycrystalline with poor <001> fiber texture. The aluminum had <111> fiber texture. Also some BaF_2.	Hysteresis loop with mercury probe. Unopened loop, low bre- akdown voltage	BMF-Si-41
BMF-Si-42	4-80-cmN/N+		900, 10 Min.	1075	550, 12 Min.	15, 0.1-0.3	350-150				R=9E50 on RT-66. No closed loop. Strange shape.	BMF-Si-42

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C),Duration	Monitor Thickns,Rate (nm),(Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Film Code
BMF-Si-43	65-95Ω-cm 2" p-Si(110)		900, 10 Min.	1085, cleaned crucible neck	550, 15 Min. True T < 350°C	12.5, 0.1-0.2	300-150		Vac-anneal 1 piece at 550°C for 30 Min.	Amorphous as grown, preferred <010> oriented after vacuum anneal. No traces of contamination.		BMF-Si-43
BMF-Si-44	0.020-cm p-Si from Monsanto		900, 10 Min.	1085	350, 14 Min.	15, 0.2-0.3	350-150		Vac-anneal pieces at 325 350,400.500,600, 700°C for1hr, 550, 600°C for 1/2hr.	Amorphous as grown. Vac-anneal different temps and times. 325°C, 350°C, 1hr, still amorphous. 400°C, 500°C, 600°C, & 700°C for 1hr, <011> multi-epi + <010> fiber structure. 600°C 30 min., more pronounced <010> fiber structure.	Narrow loop after 400 & 500 anneal, wider after higher temp anneal. No polarization loop.	BMF-Si-44
BMF-Si-45	Semi-processed #7672-5,ATL		Only degrease	1085	350, 8.5 Min.	10, 0.1-0.3	250-125		To ATL			BMF-Si-45
BMF-Si-46	#7622-6,ATL		Only degrease	1085	350, 7 Min.	10, 0.2-0.4	250-125		To ATL			BMF-Si-46
BMF-Si-47	#7622-7,ATL		Only degrease	1075	350, 11 Min.	10, 0.1-0.2	250-125		To ATL			BMF-Si-47
BMF-Si-48	#7622-8,ATL		Only degrease	1075	350, 11 Min.	10, 0.1-0.2	250-125		To ATL			BMF-Si-48
BMF-Si-49	Gridded wafer #SA-P-14		900, 10 Min.	1075	350, 11 Min.	10, 0.1-0.2	170-120		To ATL			BMF-Si-49
BMF-Si-50	2" p-Si(110)		900, 10 Min.	1085	550, 12 Min.	15, 0.1-0.3	300-150		DEKTAK- 195nm	Polycrystalline as grown, with slight <011> fiber texture.		BMF-Si-50
BMF-Si-51	2" p-Si(110)		900, 10 Min.	1085	650, 10 Min.	10, 0.1-0.3	250-125		DEKTAK- 150nm	Mostly polycrystalline with slight <010> fibe texture.		BMF-Si-51
BMF-Si-52	0.020-cm, p		900, 10 Min.	1085	375, 10 Min.	15, 0.1-0.3	300-150		2 pieces annealed in H_2 and Vac. 500°C, 1 hr.	Amorph as grown. <011> multi-epi after H_2 anneal and vacuum anneal.	Too leaky for RT-66 Narrow loop on S-T after H_2 and Vac. anneal. No hysteresis.	BMF-Si-52
BMF-Si-53	0.020-cm, p		900, 10 Min.	1085	550, 10 Min.	12.5, 0.1-0.3	250-125			Multi-epi. <011> up + some <010> fib. tex. No poly.		BMF-Si-53
BMF-CaF-Si-1	10 nm CaF_2 on .02 Ω-cm Si		900, 20 Min.	1400 (CaF_2) 1085 (BMF)	585, 3 Min. 500, 13 Min.	3, 0.1-0.2 20, 0.2-0.3	10 nm CaF_2 400-300 BMF		SiO_2 cap by PECVD	Polycrystalline		BMF-CaF-Si-1
BMF-Si-54	30 nm PtSi on Si from ATL		Only degrease	1085, add mat. to refil 1/3.	400, 16 Min.	20, 0.1-0.3	450-300			Polycrystalline with slight <010> fiber texture.	Too leaky for RT-66 R = 1E5Ω.	BMF-Si-54
BMF-Si-55	Gridded wafer #FM-N13	Fluridation	900, 20 Min.	1085	550, 8 Min.	10, 0.0-0.1	75-125 nm	None	To ATL, 7/22			BMF-Si-55
BMF-Si-56	Gridded wafer #FM-N-14	Fluoridation	900, 20 Min.	1085	350, 8 Min.	10, 0.0-0.1	75-125 nm	None	To ATL, 7/22		Excellent C-V plot a ATL with mercury probe after 500 nm SiO_2 cap by PECVD at 450°C	BMF-Si-56
BMF-Si-57	p/p+		900, 20 Min.	1085	650, 9 Min.	15, 0.0-0.1	150-900			Multiple epi with <011> up, plus unidentified phase <040>? XRD confirms confirms <011> + <010>	R = 2E6 to 2E8Ω on RT-66. No [illegible] loop. Strange.	BMF-Si-57
BMF-Si-58	0.020-cm, p	rotation probl.	900, 20 Min.	1085	150,24 Min., rotation probl.	26, 0.0-0.1	300-150		4 pieces. 60 min. vac. and H_2 anneal 2 pieces	Mostly poly with slight <010> fib. tex. after H_2 anneal, but poly with slightly more <010> fiber tex. after vac-anneal	[illegible] on RT-66. [illegible] on S-T [illegible] H_2 much [illegible] than vac.	BMF-Si-58

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C), Duration	Monitor Thickns, Rate (nm), (Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Film Code
BMF-Si-59	.020-cm, p		500, 10 Min.	1085	250, 24 Min.	25, 0.0-0.1	300-150		4-pieces. Vac, H_2, F.G e-beam SiO_2 + H_2 ann. H_2 + PECVD SiO_2	H_2, F.G. and Vac-anneal at 500°C for 1 hr. Poly film after H_2 & F.G. with some <010> fiber texture, same after vac-anneal.	Too leaky for RT-66 but excellent loop on S-T for the H_2 annealed piece, skinny loop for vac-anneal. Only C-loop after H_2 + PECVD SiO_2.	BMF-Si-59
BMF-Si-60	0.020-cm		900, 10 Min.	1085	200°C, then 600 anneal, 4 steps	20, 0.0-0.1	250-150		Cut into four pieces	<010> fiber textured film. XRD shows preferred <010>.	Too leaky for RT-66 Narrow loop on S-T bridge.	BMF-Si-60
BMF-Si-61	Gridded wafer #FM-N-25		900, 10 Min.	1085	350, 22 Min.	20, 0.0-0.1	250-150		H_2-annealed 500°C for 1 hr, then 20nmSiO_2 by e-beam evaporation		Too leaky for RT-66 before and after H_2-anneal. Conductive loop changing to hysteresi just prior to breakdown on S-T bridge. Better after SiO_2. Hysteresis and Fatigue on RT-66 with SiO_2 cap.	BMF-Si-61
BMF-Si-62	p/p+		900, 10 Min.	1085	200, 22 Min.	20, 0.0-0.1	300-150		H_2-anneal 1/4 & 1/2 piece at 500°C for 1 hr.	Polycrystalline after H_2 anneal, with some <010> fiber tex.	Conduct. loop on RT-66 after H_2-anneal. Needed conditioning for R measurement as usual.	BMF-Si-62
BMF-Si-63	p/p+		None	1085	200, 20 Min.	20, 0.0-0.1	300-150		H_2-anneal 1/4 & 1/2 piece at 500°C for 1 hr. F.G. anneal 4th quart.	Polycrystalline after H_2 anneal, with some <010> fiber tex. XRD confirms polycrystallinity.	Excellent Hysteresis on RT-66. Comparable loop on S-T at low freq. Good C-V. Conductivity proble. PECVD SiO_2 on 2n H_2-annealed piece, only C-loop	BMF-Si-63
BMF-Si-64	3"wafer#10w/SiO_2 (Lehigh)		None	1085	250, 10 Min.	10, 0.0-0.1	125-75		H_2-anneal 500°C, 1Hr. To Lehigh University		To Lehigh 8/15	BMF-Si-64
bMF-Si-65	3"wafer#9 w/SiO_2 (Lehigh)		None	1085	250, 5 Min.	5, 0.0-0.1	50-		H_2-anneal 500°C, 1Hr. To Lehigh University		To Lehigh 8/15	BMF-Si-65
BMF-Si-66	.020-cm, p		None	1085	200, 12 Min.	10, 0.0-0.1	125-75		3/4 H_2, 1/4 F. Gas anneal 500°C, 1Hr. 1/4 500Å SiO_2 PECVD 400		Narrow capacitive loop after H_2-anneal + PECVD SiO_2. Partial recovery after 2nd H_2 anneal. Worse after further H_2-anneal.	BMF-Si-66
BMF-Si-67	Gridded #FM-N-24	Fluoridation	None	1085	200, 9 Min.	10, 0.0-0.1	75-125 nm	H_2, 500°C, 1Hr	To ATL 9/13			BMF-Si-67
BMF-Si-68	Gridded w100Å SiO_2#FN-06	Degrease only	None	1085	200, 9 Min.	10, 0.0-0.1	75-125 nm	H_2, 500°C, 1 Hr	To ATL 9/13			BMF-Si-68
BMF-Si-69	p/p+	Fluoridation	None	1085	200, 10 Min.	10, 0.0-0.1	75-125 nm	H_2, 500°C, 1 Hr	To ATL 9/13			BMF-Si-69
BMF-Si-70	Gridded #FMN-17	Fluoridation	None	1085	200, 11 Min.	10, 0.0-0.1	75-125 nm	FG, 500°C, 1 Hr	To ATL 9/13			BMF-Si-70
BMF-Si-71	FM-N-18	Fluoridation	None	Gridded	200°C		50-75 nm	None	To ATL 9/13			BMF-Si-71
BMF-Si-72	7779-FMB-1	Fluoridation	None		200°C		75-125 nm	FG, 500°C, 1 Hr	To ATL 9/30			BMF-Si-72

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C), Duration	Monitor Thickns, Rate (nm), (Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Fil Co
BMF-Si-73	7779-FMB-2	Fluoridation	None		200°C		75-125 nm	FG, 500°C, 1 Hr	To ATL 9/30			BMF 73
BMF-Si-74	7779-FMB-3	Fluoridation	None		200°C		75-125 nm	FG, 500°C, 1 Hr	To ATL 9/30			BMF 74
BMF-Si-75	7779-FMB-4	Fluoridation	None		200°C		75-125 nm	FG, 500°C, 1 Hr Ramp up/down	To ATL 10/7			BMF 75
BMF-Si-76	7779-FMB-5	Fluoridation	None		200°C		75-125 nm	Ditto	Ditto			BMF 76
BMF-Si-77	7779-FMB-7	Fluoridation	None		200°C		75-125 nm	Ditto	Ditto			BMF 77
BMF-Si-78	7779-FMB-8	Fluoridation	None		200°C		75-125 nm	Ditto, followed by 50 nm RPCVD Si_3N_4 at 250°C	To ATL 10/7 Wafer cut for RPCVD coat.			BMF 78
BMF-Si-79	7779-FMB-9	Fluoridation	None		200°C		75-125 nm	FG, 500°C, 1 Hr Slow cool-down	To ATL 10/18			BMF 79
BMF-Si-80	7779-FMB-11	Fluoridation	None		200°C		75-125 nm	Ditto	Ditto			BMF 80
BMF-Si-81	7779-FMB-12	Fluoridation	None		200°C		75-125 nm	Ditto	Ditto			BMF-S 81
BMF-Si-82	7779-FMB-13	Fluoridation	600°C, 5 Min.		200°C		75-125 nm	Ditto	Ditto			BMF- 82
BMF-Si-83	7779-FMB-14	Fluoridation	600°C, 10 Min.		200°C		75-125 nm	Ditto	Ditto			BMF-S 83
BMF-Si-84	7779-FMB-15	Fluoridation	600°C, 10 Min.		200°C		75-125 nm	Ditto	To ATL 11/1			BMF- 84
BMF-Si-85	7779-FMB-17	Fluoridation	600°C, 10 Min.		200°C		75-125 nm	Ditto	Ditto			BMF- 85
BMF-Si-86	7779-FMB-18	Fluoridation	600°C, 10 Min.		200°C		75-125 nm	Ditto	Ditto			BMF-Si 86
BMF-Si-87	7779-FMB-19	Fluoridation	600°C, 10 Min.		200°C		75-125 nm	Ditto	Ditto			BMF- 87
BMF-Si-88	7779-FMB-21	Fluoridation	600°C, 10 Min.		200°C		75-125 nm	Ditto	Ditto			BMF-Si 88
BMF-Si-89	7779-FMB-22	Fluoridation	Ditto		Ditto		Ditto	Ditto	Ditto			BMF- 89
BMF-Si-90	7779-FMB-23	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si- 90
BMF-Si-91	7779-FMB-24	Fluoridation	600°C, 10 Min.		200°C		75-125 nm	FG, 500°C, 1Hr Slow Cool-down	To ATL, 11/8			BMF- 91
BMF-Si-92	7779-FMB-25	Degrease, skip RCA, HF-dip	520°C, 10 Min.		200°C		75-125 nm	FG, 480C, 1Hr Slow Cool-down	Ditto			BMF-Si- 92
BMF-Si-93	FMN-22	Ditto	600°C, 10 Min.		200°C		125-175 nm	Ditto	To ATL, 11/21			BMF-Si- 93
BMF-Si-94	FMC-N12	Fluoridation	600°C, 10 Min.		200°C		150-250 nm	Ditto	Ditto			BMF-S 94
BMF-Si-95	FMC-N11	Ditto	Ditto		Ditto		150-275 nm	Ditto	Ditto			BMF-Si 95

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C), Duration	Monitor Thickness, Rate (nm), (Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Film Code
BMF-Si-96	FMC-N21	Buffered HF, DI-H_2O, degrease, HF-dip.	520°C, 10 Min.		200°C		150-250 nm	Ditto	To ATL, 12/2			BMF-Si-96
BMF-Si-97	FMC-N23	Ditto	Ditto		Ditto		150-260 nm	Ditto	Ditto			BMF-Si-97
BMF-Si-98	FMC-N16	Ditto	Ditto		Ditto		150-225 nm	Ditto	Ditto			BMF-Si-98
BMF-Si-99	FMC-N15	Ditto	Ditto		Ditto		150-275 nm	Ditto	Ditto			BMF-Si-99
BMF-Si-100	FMC-N25	Ditto	Ditto		Ditto		150-275 nm	Ditto	Ditto			BMF-Si-100
BMF-Si-101	FMC-N20	Ditto	Ditto		Ditto		150-275 nm	Ditto	To ATL, 12/10			BMF-Si-101
BMF-Si-102	7620-6 patterned series	As above, except skip trichlor.	Ditto		Ditto		150-250 nm	Ditto	Ditto, delivered by Doug Adam			BMF-Si-102
BMF-Si-103	7620-5	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-103
BMF-Si-104	7620-2	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-104
BMF-Si-105	7620-3	As above, except use acetone in place of trichl.	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-105
BMF-Si-106	FMC-N02	Buffered HF, DI-H_2O, degrease, HF-dip.	Ditto		Ditto		150-250 nm	Ditto	Break for X-ray Poly with preferred <010>.			BMF-Si-106
BMF-Si-107	FMC-N19	Ditto	Ditto		Ditto		Ditto	Ditto	To ATL, 12/19			BMF-Si-107
BMF-Si-108	FMC-N17	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-108
BMF-Si-109	FMC-N01	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-109
BMF-Si-110	FMC-N09	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-110
BMF-Si-111	FMC-N13	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-111
BMF-Si-112	FMC-N10	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-112
BMF-Si-114	FMC-N06	Ditto	Ditto		Ditto		Ditto	Ditto	To ATL, 1/7/92			BMF-Si-114
BMF-Si-115	FMC-N08	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-115
BMF-Si-116	FMC-N18	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-116
BMF-Si-117	FMC-N05	Buffered HF, DI-H_2O, Degrease, HF-Dip	520°C, 10 Min.		200°C		150-250 nm	FG, 480°C, 1 Hr Slow cooldown	To ATL, 1/7/92			BMF-Si-117
BMF-Si-118	FMC-N07	Same, except replace trichlor with acetone.	Ditto		Ditto		Ditto	Ditto	To ATL, 1/15			BMF-Si-118
BMF-Si-119	FMC-N14	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-119
BMF-Si-120	FMC-N22	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-120
BMF-Si-121	p/p+, New material added in crucible; Fresh baked system	Ditto	Ditto		Ditto		Ditto	Ditto	Broke for X-ray Same (010) oriented poly.			BMF-Si-121
BMF-Si-122	FMC-N04	Ditto	Ditto		Ditto		Ditto	Ditto	To ATL, 1/30			BMF-Si-122

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C), Duration	Monitor Thickns, Rate (nm), (Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Film Code
BMF-Si-123	FMC-N24	Ditto, except skip 1:5 step in HF dip.	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-123
BMF-Si-124	FN-01	Ditto	Ditto		Ditto		Ditto	Ditto, except it was 2 hr anneal	To ATL, 2/4			BMF-Si-124
BMF-Si-125	FN-02	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-125
BMF-Si-126	FN-03	Back to 2-step HF-dip, with NH4F+HF 1-step.	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-126
BMF-Si-127	FN-04	Ditto	Ditto		Ditto		Ditto	F.G. 1Hr, 480°C	To ATL, 2/12			BMF-Si-127
BMF-Si-128	FN-05	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-128
BMF-Si-129	FP-01	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-129
BMF-Si-131	7806-1 (Patterned)	Back to 1-step HF-dip(1:50)	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-131
BMF-Si-132	7806-2	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-132
BMF-Si-133	7806-3	Ditto	Ditto		Ditto		Ditto	Ditto	To ATL, 2/17			BMF-Si-133
BMF-Si-134	7806-4	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-134
BMF-Si-135	7806-5	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-135
BMF-SI-136	FP-02	DITTO	DITTO		DITTO		DITTO	DITTO	TO ATL, 2/27			BMF-SI-136
BMF-SI-137	FP-03	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-SI-137
BMF-Si-138	FP-04	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-138
BMF-Si-139	FMD-23	Buffered HF, DI-H_2O, degrease (acetone in place of triclhl) 1-step HF dip (only 1:50)	520°C, 10 Min.		200°C		150-250 nm	Forming gas: 10% H_2 480°C, 1Hr Slow cool-down	To ATL, 2/27			BMF-Si-139
BMF-Si-140	FMD-06	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-140
BMF-Si-141	FMD-07	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-141
BMF-Si-142	FMD-08	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-142
BMF-Si-143	7806-6 (patterned)	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-143
BMF-Si-144	FMD-09	Ditto	Ditto		Ditto		Ditto	Ditto	To ATL, 3/6			BMF-Si-144
BMF-Si-145	FMD-10	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-145
BMF-Si-146	FMD-11	Ditto	Ditto		Ditto		180-280 nm	Ditto	Ditto			BMF-Si-146
BMF-Si-147	LE7786-01	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-147
BMF-Si-148	LE7786-04	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-148
BMF-Si-149	LE7786-05 (No silicide)	Ditto	Ditto		Ditto		Ditto	Ditto	To ATL, 3/16			BMF-Si-149

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C), Duration	Monitor Thickns, Rate (nm), (Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Film Code
BMF-Si-150	FMD-24	Ditto	Ditto		Ditto		215-330 nm	Ditto	Ditto			BMF-Si-150
BMF-Si-151	FM-N-16	Ditto	Ditto		Ditto		210-360 nm	Ditto	Ditto			BMF-Si-151
BMF-Si-152	FM-N-19	Ditto	Ditto		Ditto		270-490 nm	Ditto	Ditto			BMF-Si-152
BMF-Si-153	FM-N-20	Ditto	Ditto		Ditto		280-495 nm	Ditto	Ditto			BMF-Si-153
BMF-Si-154	FP-05	Ditto	Ditto		Ditto		180-280 nm	Ditto	Ditto			BMF-Si-154
BMF-Si-155	FMD-12	Ditto	Ditto		Ditto		250-400 nm	Ditto	To ATL, 3/25			BMF-Si-155
BMF-Si-156	FMD-13	Ditto	Ditto		Ditto		250-400 nm	Ditto	Ditto			BMF-Si-156
BMF-Si-157	FMD-14	Ditto	Ditto		Ditto		190-290 nm	Ditto	Ditto			BMF-Si-157
BMF-Si-158	FMD-15	Ditto	Ditto		Ditto		360-510 nm	Ditto	Ditto			BMF-Si-158
BMF-Si-159	FMD-16	Ditto	Ditto		Ditto		360-610 nm	Ditto	Ditto			BMF-Si-159
BMF-Si-160	FMD-17	Ditto	Ditto		Ditto		300-400 nm	Hydrogen anneal 480°C, 1Hr.	To ATL, 4/1			BMF-Si-160
BMF-Si 161	FMD-18	Ditto	Ditto		Ditto		300-200 nm	Ditto	Ditto			BMF-Si-161
BMF-Si-162	FMD-19, with 10 nm thermal SiO_2	Degrease only	Ditto		Ditto		300-200 nm	Forming gas anneal, 480°C, for 1 Hr.	Ditto			BMF-Si-162
BMF-Si-163	FMD-20, with 10 nm Thermal SiO_2	Degrease only	520°C, 10 Min.		200°C		300-200 nm	Forming gas, 480°C, 1Hr.	To ATL, 4/1			BMF-Si-163
BMF-Si-164	W-1 (p/p++)	Simplified proc w/1 step HF	520°C, 10 Min.		200°C		360-250 nm	None	To Virginia Tech for stress test			BMF-Si-164
BMF-Si-165	FMD-21	Ditto	520°C, 10 Min.		200°C (3-step) in-situ anneal at 520°C, 1Hr, after each step		360-250 nm in 3 steps of 120 nm each.	None	To ATL, 4/1			BMF-Si-165
BMF-Si-166	FMD-22	Ditto	520°C, 10 Min.		Ditto		300-200 nm	None	To ATL, 4/3			BMF-Si-166
BMF-Si-167	FMD-25, with 10nm Th SiO_2	Degrease only	Ditto		200°C		400-250 nm	FG, 480°C, 1Hr	To ATL, 4/22			BMF-Si-167
BMF-Si-168	FMC-23, with 10nmTh. SiO_2	Degrease only	Ditto		200°C		400-250 nm	Ditto	To ATL, 4/22			BMF-Si-168
BMF-Si-169	W-2, p/p+	Simplified proc w/1 step HF	Ditto		Ditto		180 nm	None	To VA. Tech. for stress, 4/20			BMF-Si-169
BMF-Si-170	7786-6 with 13.3nm Th. SiO_2	Degrease only	520°C, 20 Min.		Ditto		300-200 nm	FG, 480C, 1Hr.	To ATL, 4/22			BMF-Si-170
BMF-Si 171	FMC-N with 10nm Th. SiO_2	Ditto	520°C, 10 Min.		Ditto		300-200 nm	FG, 480°C, 1Hr	To ATL, 4/30			BMF-Si-171
BMF-Si-172	FMC-N21 with 10 nm Th. SiO_2	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-172
BMF-Si-173	FMD-01-X 13.3nmTh. SiO_2	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-173
BMF-Si-174	FMD-02-X 13.3nmTh. SiO	Ditto	Ditto		Ditto		Ditto	Ditto	Ditto			BMF-Si-174

Film Code	Wafer Code (Substrate)	Chemical Clean	Thermal Cleaning: (°C); (min.)	Source Temp (°C)	Growth Temp (°C), Duration	Monitor Thickns, Rate (nm), (Å/sec)	Thickness (nm)	Post-Anneal	Status	X-ray Results	Other Characterizations	Film Co
BMF-Si-175	High conductiv wafer.	Simplified proc w/1 step HF	None		150°C		Ditto	Various anneals H_2, vac, RTA	Local analysis			BMF-Si-175
BMF-Si-176	p/p+	Ditto	None		150°C		250-150 nm	H_2 anneal 425 to 500°C, 1 hr.	Local analysis			BMF-Si-176
BMF-Si-177	p/p+ (W3)	Ditto	520°C, 10 Min.		200°C		140-100 nm	None	To Va. Tech.			BMF-177
BMF-Si-178	FME-04	Ditto	None		150°C		300-200 nm	H_2, 480°C, 1 hr	To ATL			BMF-Si-178
BMF-Si-179	p/p+ (V4)	Ditto	520°C, 10 Min.		200°C		c. 48 nm	No.	To Va. Tech.			BMF-179
BMF-Si-180	p/p+	Ditto	520°C, 10 Min.		200°C		250-150 nm	H_2, 480°C, 1 hr	Large piece ATL			BMF-Si-180
BMF-Si-181	Va. Tech. (V-1)	Simplified Proc w/1 step HF	520°C, 10 Min.		200°C		133 - 97 nm	None	To Va. Tech.			BMF-Si-181
BMF-Si-182	Va. Tech. (V-2)	Ditto	Ditto		200°C		79 - 56 nm	None	To Va. Tech.			BMF-182
BMF-Si-183	p/p+	Ditto	Ditto		200°C		250-150 nm	H_2, 480°C, 1 hr	To ATL			BMF-Si-183
BMF-Si-184	p/p+	Ditto	Ditto		200°C		200-100 nm	H_2, 480°C, 1 hr	Local analysis			BMF-Si-184
BMF-Si-185	FMMF-02-13	Ditto	Ditto		150°C		270-150 nm	FG RTA, 600°C for 10 Seconds	To ATL			BMF-185

Appendix B: Table Summarizing Experimental C-V/ G_p-V TEST Results

Wafer #	Experiment	Test Results	Comments
7779FMB2; BMF-Si-73	Barrel Etched	Will not hold voltage, flat response, large and variable conductivity in dielectric	
7779FMB4; BMF-Si-75	Post Sputter	Dielectric blistered and peeling, does not hold voltage, no C-V data	
7779FMB14; BMF-Si-83	Broken top half of wafer Mercury probe, ~500Å LTO	Showed 12.5 volt window on ±10V sweep; (Files B14uc11 & B14uc13)	24 OCT 91
7779FMB7; BMF-Si-77	Simulated premetal Clean by 2 minute Sputter etch	± 20V sweep showed 19 - 20 Volt window; No ± 10 volt window.	
7779FMB13; BMF-Si-82	Aluminum dots and low temperature sinter in H_2/N_2 After 450°C sinter in H_2/N_2	± 20 Volt sweep showed a small window ~ 2 volts No Ferroelectric Window	
7779FMB17; BMF-Si-85	1000Å LTO	± 20V sweep gives No Window; +20 to -50V sweep shows a [illegible] window	
7779FMB22; BMF-Si-89	500Å LTO on 100nm BMF (File FMB22C5)	± 20V sweep gives 24V. window	7 NOV 91
7779FMB9; BMF-Si-79: 100nm 500Å LTO, 3KÅ TiW, Wafer cut into 4 quarters	T_{ess} Etch of TiW, Plasma Strip of Resist; (Files: B9TESPLS; B9BRLPLS)	Dot measurements showed no window. Dots tended to breakdown at 20V. Mercury Probe: ± 20V sweep showed 24.4 volt window, G_p: +25, -40μU. Dot showed no memory window and showed High conductance.	T_{ess} seems to give less leaky results than Barrel Plasma; (14 NOV 91)
	Barrel Etch TiW, Plasma Strip of Resist	Mercury Probe: ± 20V sweep showed 20 volt window: G_p = +500, -530μU	
	T_{ess} Etch TiW, Positstrip Resist(File: B9BRLPOS)	Dot breaks down at -20V. shows no window. Mercury Probe: breaks down at ± 20 volts. (Unexplained Misbehavior → Fluke)	
	Barrel Etch TiW, Positstrip Resist	Dots showed no ferroelectric window and breakdown ~ 20V. Mercury Probe: ± 20V sweep showed a 23.2 window & G_p = +630, -470μU	
	Anneal 450°C for 30 min. H_2/N_2	No significant improvement	
7779FMB18; FMF-Si-86	100Å LTO, 1000ÅFilament evaporated Al through Mask Anneal at 400°C for 30 min. in H_2/N_2	Aluminum dots showed no ferroelectric window at ± 50V. Aluminum dots showed no ferroelectric window at ± 50V. Mercury probe showed a 63 volt window at ± 50V real time sweep and a 59 volt window on C-V plot.	
7779FMB24; BMF-Si-91	500Å LTO, Full Clean	± 20V scan shows 26 volt window G_p = +5/-12μU (av. 2)	(15 NOV 91)
7779FMB25; BMF-Si-92	500Å LTO, Degrease, No RCA clean	± 20V scan show 24.8 volt window (av of 2); G_p = +30/-37 (av 2)	(15 NOV 91)
7779FMB23; BMF-Si-90	500Å LTO, 1K Al evaporated through mask from filament source	Al Dot - ± 20V scan showed 0.6 volt window. Small Indium foil electrode at ± 20V scan showed a 24.6 volt window (av. 2) (B23ind1)	(15 NOV 91)
	Silver Print deposited from cotton fiber on Q-Tip, Air dried 1½ hrs.	Silver Print ± 10V can showed a 12.3 volt window. Silver Print dots breakdown 10 to 20V.	(19 NOV 91)
	Coated 4 Al dots with silver print	Al-Ag dots showed no Ferroelectric window at ± 10V sweep. Dots broke down > 10V < 20V	(20 NOV 91)
7779FMB21; BMF-Si-88	500Å LTO Deposited then subjected to 60 min. Plasma Strip. (FILE #B21PLSTP)	± 30V C-V Scan Used To Pole Dielectric. ±20V Scan Showed Window Of 29.3 volts (av4), G_p = +6/-12 μU(av 2)	(21 NOV91)
FMN-22; BMF-Si-93	No RCA Preclean, 1kA Thick; 480°C FG Anneal, 1hr., 800Å LTO	Good Hysteresis With Memory Windows Often Exceeding the Programming Voltage. After trip to Sandia & return showed deterioration.	Pulsed CV Measurements: Hg Probe = > 6.65V Memory Window at 100μs, ±16V Needs Explanation
FMC-N12; BMF-Si-94	Complete Fluoridation Preclean; 480°C FG Anneal, 1hr., 2kÅ Thick, 800Å LTO	Good Hysteresis With Memory Windows Often Exceeding the Programming Voltage	3 Dec to STC for Retention Measurements (File # 3CN12F94A) (26 NOV 91)

Wafer #	Experiment	Test Results	Comments
FMC-N11; BMF-Si-95	Complete Fluoridation Preclean; 480°C FG Anneal, 1hr.,2.1kÅ Thick, 800Å LTO	Backsputter Premetal-Clean Ruins FEMFET Behavior OnTop Half of Wafer.Bottom Half of Wafer ±20v,-3.2/9=12.2Window.	3 Dec for TiW-Al CV Dots With Presputter Clean ♣
FN-07 (w/10nm SiO_2); BTO-4-2	5 to 8kÅ in Sweet Spot; 2 to 4kÅ beyond second interference ring, No Cap.	Very Leaky Capacitors Showing Both FE & Tunnelling/Trapping Hysteresis.	3 Dec for Al Dot Removal; 500Å LTO Deposition; Filament Masked Al Dots.
FN-07 (w/10nm SiO_2); BTO-4-2	5 to 8kÅ in Sweet Spot; 2 to 4kÅ beyond second interference ring, No Cap.	VIRGIN DOT: ±16V Sweep→1.4V Window; Showed Poling @20V giving larger window; ±20V Sweep→6.4V Window; ±10V Sweep→6.1V Window	(Files N7BT42C5 & C6 on 2 JAN 92)
FMC-N21; BMF-Si-96	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;2000Å Thick		4 Dec for 800Å LTO. The Bubble Defects Were Observed In The Film.
FMC-N23; BMF-Si-97	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;2050Å Thick	±16V Sweep→0.3V Window; ±20V Sweep→7.5V Window; ±50VSweep→53V Window;50V Seems To Partially Lock P_s;SodiumContaminatedDrngAlumDep.	4DecFor800ÅLTO.For1μ Al Shadow Dots. (Files $N23F97_{50}$ & $N23F97_{20}$ on 2 JAN 92)
FMC-N16; BMF-Si-98	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;1875Å Thick	20VsweepRepeated5x:Window=4V,7.4V,11.2V	4 Dec for 500Å LTO. For 1μ Al Shadow Dots.
FMC-N15; BMF-Si-99	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;2125Å Thick		4 Dec for 500Å LTO for FE Removal Experiments
FMC-N25; BMF-Si-100	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;2125Å Thick		4 Dec for 500Å LTO for FE Removal Experiments
FMC-N20; BMF-Si-101	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;2125Å Thick	(Files C20F96Ac & C20F96Af on 18 DEC 91)±20V Sweep→12.6V Window; ±16V Sweep→8.9VWindow; ±10V Sweep→3V Window(FilesC20f101H,M,&L->6JAN92)	11DecFor800ÅLTO&Ti WAl CV Dots With NO Presputter Clean(Mate To FMC-N11) ♣
LE7620A-6; BMF-Si-102	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;2000Å Thick		11 Dec for 800Å LTO
LE7620A-5; BMF-Si-103	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;2000Å Thick		11 Dec for 800Å LTO
LE7620A-2; BMF-Si-104	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C FG Anneal, 1hr.;2000Å Thick		11 Dec for 800Å LTO
LE7620A-3; BMF-Si-105	No RCA; Buffered HF, DI H_2O, Acetone Degrease; 480°C FG Anneal, 1hr.;2000Å Thick		11 Dec for 800Å LTO
FMC-N19; BMF-Si-107	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.	PRE SPUTTER&SINTER, ±20V.SWEEP SHOWED NO WINDOW	532Å LTO(13Jan92)
FMC-N17; BMF-Si-108	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N01; BMF-Si-109	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N09; BMF-Si-110	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N13; BMF-Si-111	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N10; BMF-Si-112	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)

Wafer #	Experiment	Test Results	Comments
FMC-N06; BMF-Si-114	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N08; BMF-Si-115	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N18; BMF-Si-116	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N05; BMF-Si-117	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FP-09; BTO-4-4 (Rotated)	PLD BTO: 500nm Center, 200nm Edge, Greenish; 18 Dec 91; 500°C Edge, 650°C Center, PRE SPUTTER ETCH.	TOP HALF OF WAFER , ±10v, Cp=155pF, Gp=1315/1320 Window=2.4/4.16=1.76v, ±5v, Window=1.62/2.2=0.58v	532Å LTO (13Jan92), Al/TiW dots, pre-sputter etch, dots Zylin/Barrel etch
FP-06; BTO-5-1 (Rotated)	PLD BTO: 250nm Center, 150nm Edge, Greenish; 2 Jan 92; 500°C Edge, 650°C Center	PROBED 5 CAPACITORS, ±20V., CONDUCTANCE OVER SCALE.	532Å LTO(13Jan92)
FP-07; BTO-5-2 (Rotated)	PLD BTO: 250nm Center, 150nm Edge, Greenish; 6 Jan 92; 500°C Edge, 650°C Center	MERCURY PROBE, ±20V. C-V WINDOW 11.6V.; ±10V. C-V WINDOW 3.8V.	532Å LTO(13Jan92)
FP-08; BTO-5-3	PLD BTO: 250nm Center, 150nm Edge, Rotating; 15 Jan 92; 550°C (readout)	MERCURY PROBE C_{MAX} 143.8pF, ±10V. SWEEP , DEP.-4.6V., ENH.2.0V., WINDOW 6.6V., G_p125\140 μ Ʊ, BREAKS DOWN AT 20V.	492Å OF LTO 20JAN92
FP-09; BTO-5-4	PLD BTO: 250nm Center, 150nm Edge, Rotating; 15 Jan 92; 500°C (readout)	HIGH CONDUCTANCE, NO WINDOW, LOOKED AT SMALL CAPACITOR DOTS	492Å OF LTO 20JAN92
FMC-N01; BTO-5-5	PLD BTO: 250nm Center, 150nm Edge, Rotating; 15 Jan 92; 450°C (readout)	BREAKSDOWN AT 20V.; NOT FERROELECTRIC	492Å OF LTO 20JAN92
FMC-N02; BTO-5-6	PLD BTO: 250nm Center, 150nm Edge, Rotating; 15 Jan 92; 450°C (readout)	Used forFE etch experiment.	492Å OF LTO 20JAN92
FMC-N07; BMF-Si-118	Buffered HF, DI H_2O, Degrease With Acetone , HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.	±20V., Gp=45μ Ʊ, Window -14.4/6=20.4 V. ±10V, Window=-8.35/1=9.35V. ±5V, Window=-3.3/-1.2=2.1V.	492Å OF LTO 20JAN92 No Preclean; 10kÅ Al evap.; A 100μs pulse change
FMC-N14; BMF-Si-119	Buffered HF, DI H_2O, Degrease With Acetone , HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.	±20V.SWEEP, NO RESPONSE	492Å OF LTO 20JAN92
FMC-N22; BMF-Si-120	Buffered HF, DI H_2O, Degrease With Acetone , HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in FG @ 480°C 1hr.		492Å OF LTO 20JAN92
FMC-N04; BMF-Si-122	2 Step chem clean	MERCURY PROBE, ±20V.SWEEP DEP.-13.2V., ENH.11.0V., WINDOW 24.2V.; G_p80/120 μƱ; ±10V.SWEEP, DEP.-16V., ENH.-2.4V., WINDOW 13.6V.	No difference between 1 step and 2 step clean
FMC-N24; BMF-Si-123	1 Step chem clean	MERCURY PROBE; ±20V. SWEEP, Gp18/25, DEP.-14V., ENH.14.4V., 28.4WINDOW	See Above
FP-10; BMF-Si-124	1 step chem clean,2 hr. anneal	MERCURY PROBE, ±20V.SWEEP ,WINDOW 22.6V., Gp65/53μƱ, NOT NORMAL DIP CURVES, IS THIS A GRIDDED WAFER? ±10V. WINDOW12.5V.	See Above
FMC-N12; BMF-Si-125	1 Step chem clean ,2 hr. anneal.	MERCURY PROBE, DOES NOT BEHAVE LIKE GRIDDED WAFER? ±20V., Gp40/68μƱ, WINDOW 18.4V.; ±10V.: Gp38/75, WINDOW8.4V.	See Above
FP03; BMF-Si-126	2 Step chem clean,2 hr. anneal.	MERCURY PROBE, DOES NOT BEHAVE LIKE GRIDDED WAFER? ±20V., Gp38/72, WINDOW17.2V.; ±10V., GP36/72, WINDOW 8.2V.	

Wafer #	Experiment	Test Results	Comments
FN-04; BMF-Si-127	2 Step chem clean,1 hr. anneal.	±20V,Gp=109/247,Cp=50/107,window=14.4;±10V,window1.8V; HgProbe: ±20V,Gp=55/63,Cp=41/72 window = 25.2, ±10V, window = 9.8V. Wafer does not behave as a gridded wafer.	9kÅ evap. Al dots. (See Comments On FP-1)
FN-05; BMF-Si-128	2 Step chem clean,1 hr. anneal.	Wafer used for FE etch experiments.	
FP-01; BMF-Si-129	2 Step chem clean;9KA Al DEPOSITED THROUGH MASK	C-V ON DOT, ±20V. Gp152/31, Cp79/100pF, WINDOW: 13.7/0.5 = 14.2V.; ±10V: -3.6/-2.4 = 1.2V.; MERCURY PROBE, ±20V: Gp122/17, Cp76.5/66.9, WINDOW -13.7/6.6= 20.3V.; -15/10 C-V, WINDOW = -10/1.3= 11.3; ±5V.,WINDOW = -2.3/0.35= 2.65; -25/20C-V, WINDOW= -19.8/7.5= 27.3	9KA AlDOTS DEPRESS MEMORY WINDOW ,INCREASE CONDUCTANCE, REQUESTED STC TO INCREASE BMF THICKNESS FROM 2KA TO 2.5/2.8 KA.
7806-1; BMF-Si-131	1 step chem clean		
7806-2; BMF-Si-132	1 step chem clean		
7806-3; BMF-Si-133	1 step chem clean		
7806-4; BMF-Si-134	1 step chem clean		Delivered to HDL
7806-5; BMF-Si-135	1 step chem clean		
FN-07; BTO-4-2	GRIDDED WAFER ,100 A SiO_2,1K A Al DOTS EVAP.	MEMORY WINDOW 6.6V.@10V.,WORKS AT 20V.&5V.	GOOD RESPONSE OVER LARGE PART OF WAFER
FN-08; BTO-4-3	GRIDDED WAFER,100 A SiO_2,10 K A Al DOTS EVAP.	MEMORY WINDOW @10v MAX 2.8 V.BTO ABOUT 20%THINNER THAN FN-07, BREAKDOWN 10 TO 20 V.	OVERALL DOES NOT LOOK TOO GOOD. ONLY SMALL PART OF WAFER HAD RESPONSE
FMD-01; BTO-6-2	GRIDDED WAFER,153 A LTO	MERCURY PROBE, ±5V., Gp 468/571 μU. WINDOW= -0.5/0.1 = 0.6V.; ±10V., Gp 500/600, WINDOW= 0/1.5 = 1.5V., Cmax 367pF.	
7806-7; BTO-6-3	LTO 161Å sub.		
FP-02; BMF-Si-136	1 step chem clean,2.5KÅ nom.	±10v, Cp= 53/86pF,Gp= 66/56 no memory window. ±20v, SONOS Type	1KÅ LTO Cap, no presputter etch no grid visible, Ti/Al/TiW dots
FP-03; BMF-Si-137	1 step chem clean	DA'd for bubbles	
FP-04; BMF-Si-138	1 step chem clean	DA'd for bubbles.	
FMD-06; BMF-Si-140	1 step chem clean		
FMD-07; BMF-Si-141	1 step chem clean		
FMD-08; BMF-Si-142	1 step chem clean		
7806-6; BMF-Si-143	1 step chem clean		
FMD-23; BMF-Si-139	1 STEP CHEM CLEAN,500C 1Hr. ANNEAL,250-150nm	Al Dot(13): Cp=196.7, Gp=43/66; ±5, =0.8, ±10=-7.4/-5= 2.4, ±20: -11.88/-0.08= 11.8. Hg C: Cp= 173.1, Gp= 81/110; ±5= 2.2, ±10: -9.2/0=9.2, ±20, broke down	
LE-7806-08; BTO-6-4	161A LTO ON Si	3 Transistors Showed no Memory @25 V.	
FMD-02; BTO-6-5	153A LTO , 550C 40MIN.	Hg Probe, breaks down at 20 V. ±10v, Gp= 30/70, window= 0.3/1.4= 1V. Cmax= 211pF, ±5V, window = -0.95/-0.4 = 0.55V, Cmax= 199pF.	BTO Deposit not uniform, spots
FMD-03; BTO -7-1	153A LTO, 550C 45 MIN.	Hg Probe; Breaks Down at 20V. ±10v.: Gp= 70/145, Window= -0.2/1.8 = 2V, Cmax= 277pF, ±5V: Window = -0.15/1.95= 2.1, Cmax= 274pF.	
FN09; BTO-4-4	Thermal Oxide 100Å	Bottom Half of Wafer; ±10v, Cp = 167pF, Gp = 1398/1375, Window = 1.2/4.3 = 3.1v, ±5v, 2.5/3.32 = 0.82v.	4KÅ Al 1.3kÅ TiW pre sputter clean dots were Zylin/Barrel etched Sinter 400 H_2/N_2
FP06; BTO-5-1	Thermal Oxide 100Å	One dot showed no window one dot showed 0.5v window, one dot non ferroelectric.	As Above
FP07; BTO-5-2	Center 2500Å, edge 1500Å, Thermal Oxide 100Å	Hg Probe: center ±20v, 11.6V window; ±10V, 3.8V window	
FMC-N-08; BTO-7-3	550 C, 40 min., 200 mTorr $10H_2$, 20 rpm.100Å Thermal Oxide	±5v, Cp = 466/451pF, Gp = 214/472. Window = 0.48/1.38 = 0.9v, ±10v, Cp = 478, Gp = 411/1146, Window = 1.2.2.9 = 1.7v.	500Å LTO no presputter, grid visible, Ti/Al/TiW dots
LE7786-02, BTO-7-2	550 C, 45 min., 200 mTorr $10H_2$, 20 rpm.LTO 187Å		

Wafer #	Experiment	Test Results	Comments
FMD-09; BMF-Si-144	2.5KÅ nom.	±10v, Cp = 130/135pF, Gp = 25/40μ Ʊ Window = -4.4/-0.8 = 3.6v ±5v, Window ≈ 0.9v	500Å LTO Cap, no presputter, grid visible, Ti/Al/TiW dots
FMD-10; BMF-SI-145	250-150nm.	Al Dot(4, 6): Cp = 164.5, Gp = 24/47; ±5, -4.2/-3.8 = 0.4, ±10, -4.3/-2.6 = 1.7, ±20, broke down, ;Hg C: Cp = 195.5, Gp = 37/69;±5, ≈2.2, ±10, -7.84/3 = 10.84, ±20, -19.2/5.2 = 24.	
FMD-11; BMF-Si-146	280-180 nm.	Al Dot(4, 6): Cp = 101.9, Gp = 11/50; ±5, ≈0, ±10, 2.2/6.0 = 3.8, -6.56/10.2 = 16.76;Hg C : Cp = 127.2, Gp = 10/31, ±5, 2.1/3.9 = 1.8, ±10, 0.5/ 7.3 = 6.8, ±20, broke down.	
LE7786-01; BMF-Si-147			
LE7786-04; BMF-Si-148			
FP-10; BTO-7-4	550°C, 10%H_2, 200 mTorr, 40min. Thermal Oxide	±5v, Cp = 128/369pF, Gp = 826/970, SONOS Type Window at±10@5 v.	500Å LTO, pre sputter etch, no grid visible, Ti/Al/TiW dots. Used in etch experiment
FMD-04; BTO-7-5	550°C, 10%H_2, 200 mTorr, 40min. Thermal Oxide; LTO suboxide	±10v, Cp = 460/440, Gp = 1179/1078, SONOS type displacement ±5v, Window ≈ 0.3v.	500Å LTO, no pre sputter etch; grid visible, Ti/Al/TiW dots. Used in etch experiment.
FMC-N-09; BTO-7-6	600°C, 10%H_2, 200 mTorr, 40min. Thermal Oxide; Thermal Suboxide	Hg Probe;Cp = 109.5pF, Gp = 68/82μƱ, ±10v = 2.7/3.76 = 1.06v, ±5v = 1.3/3.65 = 2.35v	Possible Cu Contamination
LE7786-05; BMF-Si-149			
FMD-24; BMF-Si-150	3.3KÅ nom.	±10v, Cp = 99/96, Gp = 28/48, Window = -1.24/1.84 = 3.08 ±5v, Window ≈ 2.3v.	500Å LTO Cap, no presputter, grid visible, Ti/Al/TiW dots
FM-N-16; BMF-Si-151		Wafer used for FE etch experiments.	
FM-N-19; BMF-Si-152	4.9KÅ nom,	±10v, Cp = 72/69pF, Gp = 14/153μ Ʊ. No window Can be measured, at ±20/10/5v, Too spreed out	500Å LTO, no presputter, grid visible, Ti/Al/TiW dots
FM-N-20; BMF-Si-153		Used for FE etch experiments.	
FP-05; BMF-Si-154	2.8KÅ nom.	±10v, Cp = 21/126pF, Gp = 8/102μ Ʊ, dot no window, Hg ≈ 0.8v window ±20v, Window ≈ 6.2v, Hg ≈ 6.0v.	
FMC-N-10; BTO-8-1	600°C Dep.	Hg Probe; Cp = 137pF, Gp = 101/120μ Ʊ, ±10v Window = 3.6v, ±5vWindow = 3.67v	468Å LTOCap
FMC-N-11; BTO-8-2	600°C Dep. 600°C 1 Hr Anneal	Hg Probe;Cp = 223.9pF, Gp = 63/107μ Ʊ, ±10v SONOS WINDOW, ±5vWindow = 1.1v Window, Breaks Down at20v.	468ÅLTO Cap
FMD-12; BMF-Si-155	Thickness = 350-400 nM	Al Dot(13): Cp = 82.5, Gp = 11/108; ±5, ≈2.7, ±10 = 1.6/6.5 = 4.9, ±20, -0.2/10.8 = 11;Hg C: Cp = 74.9, Gp = 41/51;±5, -0.1/2.5 = 2.6, ±10, (-0.9)/4.7 = 5.6, ±20, -5.52/9.6 = 15.1	534Å LTO, 3/27/92
FMD-13; BMF-Si-156	Thickness = 250-400nM	Used for FE etch experiment.	534Å LTO Cap, 3/27/92
FMD-14; BMF-Si-157	Thickness = 290-290 nM	Al Dot(8, 8): Cp = 136.2, Gp = 12/31; ±5, ≈0.6, ±10, ≈1.3, ±20, -14.8/ 8.2 = 23;Hg C: Cp = 72.8, Gp = 10/40; ±5, 0.4/2.15 = 1.75, ±10, (-7)/1.8 = 7.8, ±20, -16/10.2 = 26.2.	534Å LTO Cap, 3/27/92
FMD-15; BMF-Si-158	Thickness = 360-610 nM	DA'd for bubbles.	534Å LTO Cap, 3/27/92
FMD-16; BMF-Si-159	Thickness = 360 610 nM	Al Dot(12): Cp = 61.8, Gp = 11/14; ±5, ≈1.4, ±10, 1.0/8.2 = 7.2, ±20, 0/11.6 = 11.6;Hg C: Cp = 63.6, Gp = 19/ 15;±5, -1.92/1.3 = 3.2, ±10, (-1.2)/7.0 = 8.2, ±20, -8.8/9.8 = 18.6. 500 Rad Si X-Ray: Al Dot(12): Cp = 61.5, Gp = 8/11;±5, ≈1.7, ±10, 0.1/ 7.68 = 7.58, ±20, (-1.5)/13.4 = 14.9	534Å LTO Cap, 3/27/92 Conclusion of rad test at 500 Rad Si is that there was no significant change. Therefore the wafer sent to SANDIA was not damaged by airport X-ray.
FMC-N-12; BTO-8-3	300C DEP, RTA 600C, 10SEC.	±10v.Cp = 359.8pF, Gp = 334/435, Wind = 1.4/4.1 = 2.7v, ±5v, Wind = 1.35/3.05 = 1.7v.Broke Down 20v.	
FMC-N-13; BTO-8-4	300C DEP, RTA 650C, 10SEC.	±10v, Cp = 270.9, Gp = 25/101, Wind = 3.6/4.56 = 0.96v, ±5v Wind = 3 3/3.6 = 0.3v., Broke down 20v.	
FMD-17; BMF-Si-160	300-200NM, H_2, 480C, 1Hr.	Al Dot(8): Cp = 132.1, Gp = 45/75; ±5v, Wind = ≈0.25v, ±10v = 0.76/1.5 = 2.26, ±20v, -15.8/8.6 = 24.4v. Hg C: Cp = 115.5, Gp = 34/50;±5, 0.25 /1.15 = 0.9v, ±10, -1.74/2.2 = 3.94, ±20, -17/8.12 = 25.12	
FMD-18; BMF-Si-161	300-200NM, H_2, 480C, 1Hr.		
FMD-19; BMF-Si-162	Degrease Only, H_2, 480C, 1Hr., 100Å buffer oxide 300-200 nm. BMF	Al Dot(12): Cp = 105.4, Gp = 69/80; ±5, -1.8/-0.5 = 1.3, ±10, -2.5/0.98 = 3.5, ±20, -4.12/9.4 = 13.5. Hg C: Cp = 86.6, Gp = 55/50;±5, -0.6/ 0.85 = 1.45, ±10, (-1.5)/2.4 = 3.9, ±20, -5.1/10.8 = 15.9	

Wafer #	Experiment	Test Results	Comments
FMD-20; BMF-Si-163	Degrease Only, H_2, 480C, 1Hr., 100Å buffer oxide 300-200 nm, BMF		
FMD-21; BMF-Si-165	3-Step Growth, 250-360 nm.	Al Dot(4, 6): Cp = 141.5, Gp = 27/45; ±5v, Wind. = ≈0.7v, ±10v, Wind = 4.1/7.6 = 3.5, ±20v, Wind = 4.68/9.68 = 5 Hg C: Cp = 97.02, Gp = 9/18, ±5v, 2.65/4.25 = 1.6, ±10v, 1.5/5.96 = (4.46), ±20v, -15/7 = 22	
FMD-22; BMF-Si-166	3-STEP GROWTH, 300-200 NM.	Al(12), Cp = 160.3, Gp = 44/19, ±5v Wind ≈1.5v, ±10 Wind = 2.4/6.1 = 3.7, ±20v Wind = -2.8/9 = 11.8.Al(9);Cp = 148.7, Gp = 20/40, ±5v Wind ≈1.4, ±10v, Wind = 2.8/6.44 = 3.64, ±20v, Wind = -2.8/8.8 = 11.6.Hg(c);Cp = 168.7, Gp = 74/100, ±5v, Wind = -0.6/2.4 = 3.0, ±10v, Wind = -2.8/4.3 = 7.1, ±20v, -14.8/8.4 = 23.2.Hg(E); Cp = 185.4, Gp = 106/134, ±5v, Wind = -0.6/2.3 = 2.9, ±10v, Wind = (-2.44) /4.74 = 7.18, ±20v, Wind = Broke Down.	
FMC-N-14; BTO-8-5/6	RTA 600C/10SEC., 410-360 NM.	Al(4, 6);Cp = 299.6, Gp = 96/173, ±10v, Wind. = SONOS. Hg(C);Cp = 303.6, Gp = 34/97, ±5, 10, 20v, All Have SONOS response. Hg(E); Cp = 281.6, Gp = 250/294, ±5, 10, 20v All Have SONOS response.	
FMC-N-15; BTO-9-3	550C-60MIN. GROWTH	Al(4, 6);Cp = 345.6, Gp = >1.8E3, ±5, 10, 20v, Too High GP for C-V Hg(C);Cp = 118.3, Gp = 11/77, ±5v, (-1.85) /1.45 = 3.3, ±10v-0.96/2.2 = 3.16, ±20v, 2.28/4.32 = 2.0v, .Hg(E);Cp = 136.4, Gp = 14/27 ±5v, (-0.62) /2.85 = 3.47, ±10v, -0.8/2.64 = 3.44, ±20v, Broke Down	
FMC-N-16; BTO-9-4	300C-60 MIN.;RTA 600C/10SEC.	Al(12);Cp = 412.6, Gp = 539/417, ±5v, ≈0, ±10v, 4.16/4.7 = 0.54. Al(11);Cp = 423.4, Gp = 188/353, ±5v, ≈0, ±10v, 4.3/4.6 = 0.3, ±20v, SONOS. Hg(C): Cp = 321.5, Gp = 108/190, ±5v, ≈2, ±10, 20v, SONOS. Hg(E): Cp = 268.7, Gp = 319/342, ±5v, ≈2.1, ±10, 20v, SONOS.	
FMC-N-18; BTO-10-2	300C-60MIN.;RTA 550C/10SEC.	Al(4, 6);Cp = 304.6, Gp = 126/217, ±5v, 3.36/3.5 = 0.14, ±10v, 4.01/ 4.56 = 0.55, ±20v, SONOS. Hg(C): Cp = 330.7, Gp = 32/112, ±5v, ≈1.4, ±10v, 3.64/4.5 = 0.86, ±20v4.6/8.4 = 3.8.Hg(E);Cp = 298.1, Gp = 27/88, ±5v, ≈1.28, ±10, 20v, SONOS.	
FMD-25; BMF-Si-167	100ÅBuffer Oxide	Al(4, 6)Cp = 61, Gp = 10/13, ±5 = -2.45/1.2 = 3.65, ±10 = (-3.5) /3.2 = 6.7, ±20 = 5.2/10.72 = 5.52;Hg(C)Cp = 78, Gp = 6/11, ±5 = -2.55/1.92 = 4.47, ±10 = (-2.64)/4.24 = 6.88, ±20 = (-7.12)/12.48 = 19.6	
FMC-N23; BMF-Si-168	100Å Buffer Oxide		
7786-6; BMF-Si-170	133Å Buffer Oxide		
W-1; BMF-Si-164	STRESS SAMPLE 362-245nm	Deposited 500Å LTO	SENT TO VA TECH 5/1/92
FMC-N-19; BTO-10-4	550C-60min. 450nm		
FMC-N-20; BTO-11-1	DEP 300C/60min, ANNEAL 600C0.5Hr	SONOS RESPONSE	
7786-8; BTO-11-2	BUFFER 48.5nm, 550C/60min. 450 nm.		
FMC-N-22; BMF-Si-171	BUFFER 100Å TO, 300 -200nm.	Al(12) Cp = 109, Gp = 120/202, ±5 = -3.33/ (-1.3) = 2.03, ±20 = (-5.16) /2.5 = 7.66, ±20 = -5.92/10.48 = 16.4; Hg(C) Cp = 93, Gp = 6/11, ±5 = -1.1/1.69 = 2.79, ±10 = (-3.2) /5.38 = 8.58, ±20 = -9.2/12.08 = 21.28	
FMC-N-21; BMF-Si-172	BUFFER 100Å TO, 300 -200nm.		
FMD01X; BMF-Si-173	BUFFER 135Å TO, 300 -200nm.	Al(4, 6)Cp = 80.7, Gp = 3/7, ±5 = -3.35/-1.35 = 2.0, ±10 = -5.1/1.9 = 7.0, ± 20 = -8.32/8.88 = 17.2; Al(4, 4): Cp = 67.6 Gp = 4/8, ±5 = -3.12/-1.2 = 1.92, ±10 = -5.1/1.9 = 7.0, ± 20 = -8.56/8.96 = 17.52; Hg(C): Cp = 92, Gp = 4/10, ±5 = -2.02/1.4 = 3.4, ±10 = -3.84/4.2 = 8.04, ± 20 = -8.76/11.4 = 20.16; Hg(ES): Cp = 88, Gp = 5/11, ±5 = -0.15/2.1 = 2.25, ±10 = -2.0/7.1 = 9.1, ± 20 = -9/11 = 20.0	
FMD02X; BMF-Si-174	BUFFER 135Å TO, 300 -200nm.	Al(4, 6) Cp = 81, Gp = 3/7, ±5 = -3.35/-1.35 = 2.0, ±10 = -5.1/1.9 = 7.0, ±20 = -8.32/8.88 = 17.2;Hg(C) Cp = 92, Gp = 4/10, ±5 = -2.02/1.4 = 3.4, ±10 = -3.84/4.2 = 8.04, ±20 = -8.76/11.4 = 20.16.	
LE7786-07; BTO-11-3	550C/30MIN. STATIC RUN, 242Å TO BUFFER		

Wafer #	Experiment	Test Results	Comments
FMD14X; BTO-11-4	550C/60MIN., 20RPM, TO = 506Å	Al(4, 4)Cp = 173, Gp = 24/60, ±5 = 0.45, ±10 = 0.9, ±20 = -2.72/-0.96 = 1.76 Hg(ES)Cp = 98, Gp = 9/18, ±5 = -2.18/-0.82 = 1.36, ±10 = -2.3/-0.2 = 2.1, ±20 = -3.2/-0.3 = 2.9	
FMD-08X; BTO-12-1	550C/60MIN., 20RPM, TO = 256Å	Al(12) Cp = 358, Gp = 170/294, ±5 = -2.39/-1.86 = 0.53, ±10 = -2.34/-1.08 = 1.26, ±20 = -1.28/0.8 = 2.08, Hg(EE) Cp = 98, Gp = 10/18, ±5 = -2.9/-1.7 = 1.2, ±10 = -3.6/-0.8 = 2.8, ±20 = -5.2/2.3 = 7.5,	
W-2; BMF-Si-169	Va. TECH. STRESS MEAS.	SENT TO Va.TECH 5/22/92	700Å LTO CAP
FMD-09X; BTO-12-2	550C/60MIN., 20RPM, TO = 256Å	Ti(4, C): Cp = 225/222, Gp = 41/94, ±5 = ≈1.1, ±10 = -1.2/0.52 = 1.72, ±20 = -0.3/3.6 = 3.9, ;Ti(4EW): Cp = 221/218, Gp = 45/103, ±5 = 0.38/0.1 = 0.48, ±10 = (-0.6)/0.36 = 1.0, ±20 = 0.2/2.8 = 2.6; Hg(CC): Cp = 157/137, Gp = 102/376, ±5 = -0.05/0.1 = 0.15, ±10 = 0.1/0.2 = 0.3, ±20 = (-0.2)/0.6 = 0.8, ; Hg(EE): Cp = 137/134, Gp = 65/51, ±5 = -0.2/0.42=0.62, ±10=(-0.26)/0.72= 0.98, ±20=0.2/1.8= 1.6; Hg(EW): Cp=119/114, Gp = 13/70, ±5 = 0.35/1.65 = 2.0, ±10 = 0.66/1.9 = 1.24, ±20 = -0.8/0.2 = 1.0;	
FMD-15X; BTO-12-3	550C/60MIN., 20RPM, TO = 506Å, 50mTORR	Ti(4, C): Cp = 146/149, Gp = 38/60, ±5 = ≈0.1, ±10 = -2.7/-1.9 = 0.8, ±20 = -3.2/(-0.6) = 2.6; Ti(4EW): Cp = 130/148, Gp = 84/58, ±5 = 0, ±10 = 0, ±20 = ≈0.4;Ti(4, EE): Cp = 75/147, Gp = 41/54, ±5 = 0, ±10 = 0, ±20 = 0;Hg(CC): Cp = 119/126, Gp = 41/42, ±5 = SONOS, ±10 = SONOS, ±20 = SONOS; Hg(EW): Cp = 115/118, Gp = 20/30, ;±5 = ≈0.6, ±10 = ≈1.2, ±20 = -4.4/(-2.2) = 2.2; Hg(EE): Cp = 100/106, Gp = 31/28, ±5 = ≈0.5, ±10 = ≈1.2, ±20 = -4.72/ (-1.2) = 3.52	
FMD-16X; BTO-12-4	510/60MIN., 20RPM, TO = 506Å, 50mTORR		
FMD-10X; BTO-13-1	490C/60MIN., 20RPM, TO = 256Å, 50mTORR	Al(4, 6): Cp = 203/204, Gp = 51/60, ±5 = -2.88/-1.4 = 1.48, ±10 = -3.2/ (-2.0) = 1.2, ±20 = -4.4/-2.56 = 1.84; Al(4, 4): Cp = 191/191, Gp = 27/64, ±5 = -2.7/-2.2 = 0.5, ±10 = -2.96/-1.8 = 1.16, ±20 = -2.8/(-1.2) = 1.6; Hg(CC): Cp = 146/145, Gp = 16/35, ±5 = -2.8/-1.4 = 1.4, ±10 = (-3.24)/(-0.64 = 2.6, ±20 = Broke Down; Hg(ES): Cp = 158/154, Gp = 18/39, ±5 = -4.2/-3.4 = 0.8, ±10 = -5.6/-1.56 = 4.04, ±20 = (-8.2)/5.2 = 13.4;Hg(EE): Cp = 147/142, Gp = 34/51, ±5 = -2.92/-1.42 = 1.5, ±10 = (-3.9)/-0.5 = 3.4, ±20 = -4.88/0.88 = 5.76	
FMD-11X; BTO-13-2	510C/30MIN., 20RPM, TO = 256Å	Al(4, 6): Cp = 239/238, Gp = 40/99, ±5 = -2.8/-1.9 = 0.9, ±10 = -3.1/-1.3 = 1.8, ±20 = (-2.2)/0.6 = 2.8; Al(4, 4): Cp = 241/240, Gp = 44/103, ±5 = ≈0.8, ±10 = -2.9/-1.4 = 1.5, ±20 = (-2.32)/0 = 2.32; Hg(CC): Cp = 126/122, Gp = 12/26, ±5 = -3.9/-3.1 = 0.8, ±10 = -4.6/-1.8 = 2.8, ±20 = (-8)/-1.2 = 6.8; Hg(EN): Cp = 103/95, Gp = 3/12, ±5 = -2.93/(-0.05) = 2.88, ±10 = -3.36/0.6 = 3.96, ±20 = -2.72/(-0.2) = 2.52; Hg(EE): Cp = 112/105, Gp = 10/19, ±5 = -2.2/-0.4 = 1.8, ±10 = -2.6/0 = 2.6, ±20 = (-2.4)/0.6 = 1.8; Hg(EW): Cp = 92/81, Gp = 5/10, ±5 = ≈1.5, ±10 = -4.76/-1.56 = 3.2, ±20 = (-8.4)/(-0.8) = 7.6;Hg(ES): Cp = 140/121, Gp = 14/22, ±5 = (-2.28)/0.62 = 1.66, ±10 = -2.36/-0.2 = 2.16, ±20 = -3.28/0.32 = 3.6	
FMD13X; BTO-13-4	490C/20MIN, 256Å BUFFER	Al(3, 12): Cp = 310/312, Gp = 38/142, ±5 = -3.0/-2.7 = 0.3, ±10 = -3.2/-2.4 = 0.8, ±20 = -3.8/-1.6 = 2.2;Al(3, 9): Cp = 338/339, Gp = 53/171, ±5 = -3.0/-2.65 = 0.35, ±10 = -3.24/-2.36 = 0.88, ±20 = -4.2/-1.4 = 2.8, ;Al(6, 11): Cp = 73/65, Gp = 59/173, ±5 = -3.1/ 2.65 = 0.45, ±10 = -3.5/-2.24 = 1.26, ±20 = -4.72/-1.16 = 3.56; Hg(CC): Cp = 73/65, Gp = 8/11, ±5 = -3.9/-1.6 = 2.3, ±10 = -4.8/-0.3 = 4.5, ±20 = -6.32/2.0 = 8.32; Hg(ES): Cp = 73/63, Gp = 8/11, ±5 = -4.4/-2.6 = 1.8, ±10 = -4.84/-0.64 = 4.2, ±20 = -8.6/0.4 = 9.0; Hg(EW): Cp = 138/128, Gp = 112/111, ±5 = -2.55/-0.62 = 1.93, ±10 = -2.98/-0.1 = 2.88, ±20 = -3.6/0 = 3.6;	
FMD03; BTO-13-5	510C/20MIN, 135Å BUFFER	Al(12): Cp = 409/404, Gp = 113/254, ±5 = -2.23/-1.38 = 0.85, ±10 = -2.26/-0.8 = 1.46, ±20 = BrokeDown, ;Al(9): Cp = 406/402, Gp = 109/248, ±5 = -2.3/-1.45 = 0.85, ±10 = -2.38/0.84 = 1.54, ±20 = BrokeDown;Al(2, 13): Cp = 401/397, Gp = 106/245, ±5 = -2.3/-1.4 = 0.9, ±10 = -2.3/0.8 = 1.5, ±20 = BrokeDown;Hg(CC): Cp = 110/97, Gp = 42/43, ±5 = -1.35/-0.4 = 0.95, ±10 = 1.4/-0.2 = 1.2, ±20 = BrokeDown;Hg(ES): Cp = 101/86, Gp = 12/16, ±5 = -1.68/-0.32 = 1.36, ±10 = -2.0/0 = 2.0, ±20 = Broke Down;	

Wafer #	Experiment	Test Results	Comments
FMD-04X; BTO-14-1	550°C/20 MIN.;135Å BUFFER, 10K Al 150°C Dep &Photo Lith.	Al(C): Cp = 284/280, Gp = 42/145, ±5 = 0.1, ±10 = 1.0/1.36 = 0.36, ±20 = SONOS;Al(ES): Cp = 293/288, Gp = 47/154, ±5 = 0.1, ±10 = 1.2/1.6 = 0.4, ±20 = SONOS;Al(EN): Cp = 283/277, Gp = 47/157, ±5 = 0.1, ±10 = 0.1, ±20 = 4.8/6 = 1.2;Hg(ES): Cp+314/307, Gp = 66/146, ±5 = 0.05/0.72 = 0.67, ±10 = 0/0.7 = 0.7, ±20 = SONOS;Hg(CC): Cp = 189/184, Gp = 24/59, ±5 = SONOS, ±10 = SONOS, ±20 = SONOS.	
FMD-05X; BTO-14-3	550°C/30 MIN.,135ÅBUFFER ;NO ROTATION;277 nm AT EDGE, 200mTORR	Al(4, 9): Cp = 384/374, Gp = 217/341, ±5 = -1.18/0.35 = 1.53, ±10 = -1.3/0.7 = 2.0, ±20 = 0.6/2.32 = 1.72;Al(6, 6): Cp = 438/425, Gp = 195/352, ±5 = -0.25/0.75 = 1.0, ±10 = -0.3/1.08 = 1.38, ±20 = SONOS, Al(3, 12): Cp+393/384, Gp = 154/294, ±5 = -0.87/0.65 = 1.52;±10 = -1.2/1.2 = 2.4, ±20 = SONOS; Hg(1R): Cp = 107/99, Gp = 182/168, ±5 = 0, ±10 = SONOS; Hg(2R): Cp = 249/149, Gp = 229/39, ±5 = -0.7/1.8 = 2.5, ±10 = -0.96/2.3 = 3.28, ±20 = 0;Hg(3R): Cp = 142/140, Gp = 17/36, ±5 = -3.1/2.1 = 5.2, ±10 = -0.8/1.6 = 2.4, ±20 = Break Down.	
FMD-06X; BTO-14-4	550°C/30 MIN.;135ÅBUFFER;NO ROTATION;500mTorr	Al(4, 4): Cp = 338/328, Gp = 58/238, ±5 = 0.2/1.52 = 1.32, ±10 = SONOS;Al(4, 5): Cp+321/ 308, Gp+58/354, ±5 = 0.3/1.45 = 1.15, ±10 = SONOS;Al(4, 2): Cp+321/314, Gp = 74/189, ±5 = 0.6/1.0 = 0.4, ±10 = SONOS;Hg(1R): Cp = 74/63, Gp = 30/11, ±5 = SONOS, ±10 = SONOS; Hg(2R): Cp+86/79, Gp = 8/72, ±5 = 0.7, ±10 = 2.6/5.8 = 3.2, ±20 = SONOS; Hg(3R): Cp = 131/ 122, Gp+15/47, ±5 = 0.22/1.08 = 0.86, ±10 = 0.56/1.26 = 0.7, ±20 = Broke Down.	
FMD-07X; BTO-14-5	550°C/30 MIN.;135Å BUFFER;NO ROTATION;10 mTorr	Al(12, 13): Cp+315/311, Gp = 122/226, ±5 = -1.35/-1.15 = 0.2, ±10 = -4.01/0.2 = 4.21, ±20 = -1.52/1.8 = 3.32;Al(18, 12): Cp+319/314, Gp = 177/275, ±5 = -1.65/-0.5 = 1.15, ±10 = -3.9/0.76 = 4.66, ±20 = -3.8/1.8 = 5.6;Al(12, 14): Cp = 322/319, Gp = 104/215, ±5 = -1.48/-1.34, ±10 = -3.5/-0.9 = 2.6, ±20 = -2.92/2.4 = 5.32;Hg(R): Cp+170/168, Gp = 31/62, ±5 = -2.05/-0.85 = 1.2, ±10 = -3.7/0.7 = 4.4, ±20 = -2.2/1.2 = 3.4;Hg(G): Cp+111/97, Gp+18/21, ±5 = -1.85/0.85 = 2.7, ±10 = -3.3/2.0 = 5.3, ±20 = -3.6/1.8 = 5.4; Hg(Y): Cp+150/142, Gp+27/46, ±5 = -2.25/-1.25 = 1.0, ±10 = -4.4/-0.8 = 3.6, ±20 = -1.1.8/1.0 = 2.8;	
FMD-19X; BTO-15-1	550°C/30 MIN.;506Å BUFFER;NO ROTATION;50mTorr	Al(3, 10): Cp = 165/165, Gp = 29/57, ±5 = -3.1/-2.45 = 0.65, ±10 = -3.41/-1.83 = 1.52, ±20 = -2.88/-1.0 = 1.88;Al(3, 7): Cp = 144/102, Gp = 24/229, ±5 = -3.3/-2.9 = 0.4, ±10 = -3.7/-2.4 = 1.3, ±20 = -4.32/-1.52 = 2.8;Hg(2R): Cp = 133/131, Gp = 14/29, ±5 = -2.28/-1.78 = 0.5, ±10 = -2.5/-1.56 = 0.94, ±20 = -3.8/-1.2 = 2.6; Hg(4R): Cp = 133/128, Gp = 24/41, ±5 = -2.38/-1.94 = 0.44, ±10 = -2.6/-1.76 = 0.84, ±20 = -1.4/-1.0 = 3.4.	
FMD-20X; BTO-15-2	550°C/30 MIN.;487Å LTO BUFFER;NO ROTATION;200mTorr	Al(9, 12): Cp = 285/285, Gp = 48/124, ±5 = 0.15, ±10 = 0.4, ±20 = -3.12/-1.8 = 1.32; Al(5, 12): Cp = 279/278, Gp = 47/125, ±5 = 0, ±10 = 0.2, ±20 = 0.4;Hg(2R): Cp = 117/114, Gp = 20/21, ±5 = -1.58/-1.05, ±10 = -1.7/-1.0 = 0.7, ±20 = -2.6/-1.0 = 1.6;Hg(G): Cp = 199/ 191, , Gp = 132/159, ±5 = -1.65/-1.20 = 0.45, ±10 = -2.0/1.0 = 1.0, ±20 = -2.72/0 = 2.72	
FMD-21X; BTO-15-3	550°C/40 MIN.;487 LTO BUFFER;NO ROTATION;200mTorr	Al(3, 20): Cp = 249/247, Gp = 22/76, ±5 = 0.3, ±10 = -2.1/-1.4 = 0.7, ±20 = -2.48/-0.4 = 2.08 Al(3, 16): Cp = 285/283, Gp = 34/108, ±5 = 0, ±10 = 0, ±20 = 0;Hg(1R): Cp = 196/183, Gp = 141/102, ±5 = -1.15/-0.65 = 0.5, ±10 = -1.4/-0.44 = 0.96, ±20 = -2.4/0 = 2.4; Hg(1B): Cp = 187/176, Gp = 52/81, ±5 = 0.3, ±10 = -1.44/-0.6 = 0.84, ±20 = Broke Down.	
FMD-23X; BTO-15-4	550°C/30 MIN.;487ÅLTO BUFFER;NO ROTATION;200mTorr	Al(7, 5): Cp = 238/237, Gp = 30/73, ±5 = 0.25, ±10 = -2.3/-1.64 = 0.66, ±20 = -3.4/-2.08 = 1.32;Al(5, 5): Cp = 250/249, Gp = 38/92, ±5 = 0.4, ±10 = -2.4/-1.76 = 0.64, ±20 = Broke Down;Hg(2R): Cp = 89/80, Gp = 12/15, ±5 = -2.2/-1.6 = 0.6, ±10 = -2.4/-1.5 = 0.9, ±20 = -2.72/-1.4 = 1.32;Hg(3R): Cp = 121/116, Gp = 74/81, ±5 = 0.5, ±10 = -1.2/-0.16 = 1.04 ±20 = -1.96/1.2 = 3.16	
FMD-24X; BTO-15-5	650°/550°C/25 MIN.;487ÅLTO BUFFER;NO ROTATION;200mTorr	Al(4, 9): Cp = 221/220, Gp = 43/95, ±5 = 0.1, ±10 = 0.2, ±20 = 0.4;Al(5, 7): Cp = 238/237, Gp = 47/105, ±5 = 0.1, ±10 = 0.2, ±20 = 0.4;Hg(2R): Cp = 103/101, Gp = 28/37, ±5 = -1.4/-0.5 = 0.9, ±10 = -1.44/0.4 = 1.04, ±20 = -1.6/0 = 1.6,Hg(3R): Cp = 130/127, Gp = 32/47, ±5 = -1.62/-0.9 = 0.72, ±10 = -1.7/-0.8 = 0.9, ±20 = -2.0/-0.48 = 1.52;	

Wafer #	Experiment	Test Results	Comments
FMD 25X; BTO-16-1	550°C/30 MIN., NO BUFFER;0 RPM 7 KÅ Al Dots	Al(G): Cp = 265/264, Gp = 570/566, ±10&±20 Flat No FERROELECTRIC BEHAVIOR;Al(P): Cp = 345/343, Gp = 825/811, NO FERROELECTRIC RESPONSE;Hg(G): Cp = 229/228, Gp = 707/707, NO FERROELECTRIC RESPONSE;	
FME 01; BTO-15-2	550°C/30 MIN., NO BUFFER; 0 RPM, 1KÅ Al Dots >	±10;Cp = 357/355, Gp = 176/170, N) Ferroelectric Response At ±10 V& ±20 V, Broke Down At -40 V.	
FME 02; BTO-16-4	470°C/20 MIN., BUFFER 200Å TO, 20 RPM, 200mTorr	Al(4, 6): Cp = 152/225, Gp = 42/79, ±5 = 1.3, ±10 = 3.5, ±20 = 3.6; Al(4, 4): Cp = 117/184, Gp = 28/57, ±5 = 1.4, ±10 = 2.6, ±20 = 3.6; Hg(CC): Cp = 132/115, Gp = 109/86, ±5 = 1.6, ±10 = 1.7, ±20 = 3.6; Hg(ES): Cp = 74/62, Gp = 9/7, ±5 = 1.4, ±10 = 4.2, ±20 = 19.6.	
FME 03; BTO-16-5	450°C/20 MIN., BUFFER 200Å TO, 20 RPM, 200mTorr	Al(12): Cp = 141/258, Gp = 25/76, ±5 = 1.3, ±10 = 3.5, ±20 = 7.12; Al(9): Cp = 146/251, Gp = 31/80, ±5 = 1.5, ±10 = 3.7, ±20 = 7.2; Hg(CC): Cp = 128/172, Gp = 92/37, ±5 = 1.7, ±10 = 2.8, ±20 = 3.4; Hg(ES): Cp+105/166, Gp = 17/33, ±5 = 2.3, ±10 = 4.5, ±20 = 3.6;	
------; BTO-16-3	550°C/30 MIN., NO BUFFER, 0 RPM	±10 V, Cp = 459/26, Gp = 175/3, Al(4, 15): SONOS;Al(9, 18): ±10 = 0.76, ±20 = SONOS.	
MVE-100PO6	SPUTTERED BTO, Rm.Temp.120 W, 20μ, 3Hr , ANNEALED 650°C	±10 V;Cp = 514/18, Gp = 543/14, Al(4, 7) &Al(4, 9) Dots SHOWED NO FERROELECTRIC RESPONSE.	
FME-08; PZT-01-1	TO(10), N(40), PZT, 550°C/30 MIN., 300mTORR, RPM 0, 1 KÅ Al	Al(5, 11): Cp = 59/72, Gp = 11/13, ±5 = =0.6, ±10 = 1.9, ±20 = 2.2; Al(8, 14): Cp = 51/59, Gp = 9/11, ±5 = 0.35, ±10 = 1.3, ±20 = 2.4; Hg(1B): Cp = 46//48, Gp = 10/12, ±5 = 1.3, ±10 = 2.3, ±20 = 2.2; Hg(2B): Cp = 62/69, Gp = 9/10, ±5 = 0.6, ±10 = 1.7, ±20 = 2.0;	
FME-09; PZT-01-2	TO(10), N(40), PZT 550°C/30 MIN., 300mTORR, RPM 0	Al(A): Cp = 61/61, Gp = 129/232, ±5 = 0.1, ±10 = 0.3, ±20 = Broke Down, Al(B): Cp = 61/59, Gp = 140/464, ±5 = 0, ±10 = 0.2, ±20 = Broke Down; Hg(C): Cp = 52/52, Gp = 6/8, ±5 = 0.7, ±10 = 2, ±20 = 0/2.6 = 2.6, Hg(E): Cp+50/50, Gp = 6/8, ±5 = 0.7, ±10 = 2.2, ±20 = 0/2.88 = 2.88.	
FME-10; PZT-01-3	TO(10), N(40), PZT 550°C/40 MIN. , 300mTORR, RPM 20,	Al(8, 9): Cp = 46/56, Gp = 5/7, ±5 = 0.45, ±10 = 1.8, ±20 = 2.8; Al(3, 6): Cp = 60/66, Gp = 9/10, ±5 = 0, ±10 = 1.1, ±20 = 2.4; Hg(C): Cp = 27/36, Gp = 6/3, ±5 = 1.5, ±10 = 3.4, ±20 = 6.8; Hg(ES): Cp = 41/42, Gp = 4/4, ±5 = 0, ±10 = 3.0, ±20 = 4.6;	
FME-11; PZT-01-4	TO(10), N(40), PZT 500°C/40 MIN. 300 mTORR , RPM 20	Al(4, 6): Cp = 40/68, Gp = 12/7, ±5 = 0.6, ±10 = 1.6.±20 = SONOS, Al(3, 5): Cp = 46/61, Gp = 6/8, ±5 = 0.6, ±10 = 1.4, ±20 = SONOS, Hg(C): Cp = 38/52, Gp = 32/4, ±5 = 2.2, ±10 = 4.5, ±20 = 6.2; Hg(ES): Cp = 46/53, Gp = 4/5, ±5 = 2.2, ±10 = 3.8, ±20 = 4.8.	
FME-04; BMF-Si-178	DEP 150°C, 3000Å, ANNEAL 480°C 1 KÅ Al Dots.	Al(4, 6): Cp = 58/81, Gp = 12/14, ±10 = 2.0, ±20 = 6;Al(4, 4): Cp = 65/87, Gp = 13/15, ±10 = 1.4, ±20 = 3.2;Hg(C): Cp = 56/97, Gp = 33/53, ±5 = 2.5 ±10 = 3.4, ±20 = 6.8;Hg(ES): Cp = 65/82, Gp = 16/21, ±5 = 1.9, ±10 = =3.1, ±20 = 8.2;	
FMD-12X; BTO-13-3	510°C/20 MIN., 256Å BUFFER TO, 200mTorr, 20 RPM, 450nM BTO	Al(4, 12): Cp = 284/286, Gp = 42/129, ±5 = =0.2, ±10 = -2.8/-1.9 = 0.9, ±20 = -2.4/-0.2 = 2.2, ;Al(4, 9): Cp = 287/288, Gp = 42/128, ±5 = =0.2, ±10 = -2.8/-2.6 = 0.7, ±20 = -2.6/-0.6 = 2.0, Al(1, 10): Cp = 283/285, Gp = 43/126, ±5 = =0.2, ±10 = -2.6/-1.6 = 1.0, ±20 = -2.48/-0.08 = 2.4, ;Hg(CC): Cp = 148/123, Gp = 111/26, ±5 = -1.98/-1.02 = 0.96, ±10 = -2.2/-0.7 = 1.5, ±20 = -2.32/-0.2 = 2.12, ,Hg(ES): Cp = 116/111, Gp = 12/21, ±5 = =1.1, ±10 = -4.7/-1.8 = 2.9, ±20 = -7.6/-0.88 = 6.8, ;Hg(EN). Cp = 118/117, Gp = 164/161, ±5 = -1.85/0.82 = 1.06, ±10 = -2.04/-0.6 = 1.44, ±20 = -2.4/-0.48 = 1.92;	
P+/P+; BMF-Si-182	DEP 200°C, 2500Å, ANNEAL 480°C IN H_2, 1 KÅ Al Dots	Al(C): Cp = 78/87, Gp = 160/148, ±10 = FLAT, ±20 = 6.4, Al(E): Cp = 76/85, Gp = 157/144, ±10 = FLAT, ±20 = 4.88, Hg(C): Cp = 66/80, Gp = 110/116, ±5 = 0.7, ±10 = 1.5, ±20 = -16/3.4 = 19.4;Hg(EN): Cp = 72/85, Gp = 131/130, ±10 = 1.2, ±20 = -17.7/-2.6 = 15.2.	
P+/P+; BMF-Si-180	LARGE PIECE, BEST POLY, 200°C, 2800Å, ANNEAL H_2, 1 KÅ Al Dots.	Al(A): Cp+105/40, Gp = 15/5, ±10&20 = FLAT;Al(B): Cp = 47/50, Gp = 30/27, ±10&20 = FLAT;Hg(C): Cp = 72/54, Gp = 32/40, ±5 = 0.6, ±10 = 1.3, ±20 = 12.4;Hg(EN): Cp = 58/59, Gp = 35/73, ±5 = 0, ±10 = 1.0, ±20 = 10.8.	

Wafer #	Experiment	Test Results	Comments
FME-15;BTO-17-1 [383-102]	200ÅTO, 470 C°/19 MIN., 20 RPM, 10 mTORR	Al(9, 10): Cp = 68/227, Gp = 31/63, ±5 = 0.25, ±10 = 1.7, ±20 = 3.5; Al(9, 7): Cp = 137/242, Gp = 28/75, ±5 = 0.2, ±10 = 0.6, ±20 = 2.5; Hg(CC): Cp = 84/142, Gp = 55/233, ±5 = 0.4, ±10 = 2.7, ±20 = 8.0; Hg(ES): Cp = 100/205, Gp = 43/136, ±5 = 0.5, ±10 = 2.9, ±20 = 10.2;	
FME-16;[383-103] BTO-17-2	200 Å TO, 450°C/30 MIN, 0 RPM, 10 mTORR.	Al(2, 10): Cp = 208/207, Gp = 37/69, ±5 = -2.68/-2.38 = 0.3, ±10 = -2.7/ -1.6 = 1.1, ±20 = -10.72/-4.48 = 6.24; Al(2, 9): Cp = 181/181, Gp = 32/58, ±5 = 0.15, ±10 = -5.4/-3.2 = 2.2, ±20 = -10.0/-2.88 = 8.12;Hg(EN, G): Cp = 204/199, Gp = 189/216, ±5 = 0.25, ±10 = -4.44/-1.7 = 2.74, ±20 = -7.4/2.4 = 9.8;Hg(EN, B): Cp = 211/208, Gp = 31/63, ±5 = 0.3, ±10 = -5.96/-3.1 = 2.65, ±20 = -9.4/-0.2 = 9.2;	
FME-17;[383-104] BTO-17-3	200 Å TO, 450°C/30 MIN, 0 RPM, 10 mTORR.	Al(3, 14): Cp = 238/237, Gp = 27/68, ±5 = -4.77/-4.52 = 0.25, ±10 = -5.36/-3.84 = 1.52, ±20 = -10.72/-4.48 = 6.24;Al(4, 12): Cp = 256/255, Gp = 43/89, ±5 = 0.18, ±10 = -3.9/-2.3 = 1.6, ±20 = -6.56/-2.08 = 4.48;Hg(G): Cp = 86/80, Gp = 21/23, ±5 = -1.4/-1.18 = 0.22, ±10 = -3.1/0 = 3.1, ±20 = -6.2/5.0 = 11.2;Hg(P): Cp+163/158, Gp = 25/44, ±5 = 0.1, ±10 = -1.44/-0.8 = 0.64, ±20 = -6.2/1.4 = 7.6;	
FME-18;BTO-17-4	200Å TO, 450°C/30 MIN, 0 RPM 50 mTORR.	Al(5, 2): Cp = 269/266, Gp = 58/115, ±5 = -1.5/-0.75 = 0.75, ±10 = SONOS, Al(5, 4): Cp = 264/263, Gp = 55/113, ±5 = -2.35/ -1.65 = 0.7, ±10 = -2.7/-1.0 = 1.7, ±20 = BROKE DOWN; Al(3, 2): Cp = 266/264, Gp = 59/115, ±5 = -1.85/-1.0 = 0.85, ±10 = SONOS, Hg(2R): Cp = 88/83, Gp = 49/50, ±5 = -0.86/-0.1 = 0.76, ±10 = SONOS, Hg(3R): Cp = 182/165, Gp = 114/120, ±5 = -1.58/-0.65 = 0.93, ±10 = -1.78/-0.5 = 1.28, ±20 = BROKE DOWN;	
LE7786-09;BTO-18-1	200ÅTO, 450°C/20 MIN., 200mTORR 20 RPM.		ION MILLED AT STC
LE7786-10; BTO-18-2	200Å TO, 450 °C/20 MIN., 50m TORR, 20 RPM.	(4, 9): Cp = 199/186, Gp = 240/314, ±5 = -0.4/1.05, ±10 = -0.76/1.6 = 2.36, ±20 = 1.28/5.2 = 3.92; (4, 7): Cp = 200/196, Gp = 253/283, ±5 = 0/1.15, ±10 = -0.36/1.76 = 2.12, ±20 = 1.92/5.68 = 3.76; (3, 6): Cp = 201/198, Gp = 201/229, ±5 = 0.65/1.65 = 1.0, ±10 = -0.1/2.3 = 2.4, ±20 = 2.88/7.0 = 4.12.	ION MILLED AT STC
FME-19;BTO-18-3	550°C/20 MIN. 50 mTorr, 300°C/3 MIN. 200mTorr, 20 RPM.	Hg(CC): Cp = 116/111, Gp = 18/24, ±5 = -0.3/0.05 = 0.35;±10 = 0.2, ±20 = SONOS;Hg(EN): Cp = 146/141, Gp = 114/125, ±5 = -0.25/0.05 = 0.3, ±10 = 0.05, ±20 = SONOS;Hg(ES): Cp = 89/141, Gp = 45/95, ±5 = 0.4, ±10 = 0.2, ±20 = SONOS.	
FME-20;BTO-18-4	550°C/20 MIN., 10 mTORR, 20 RPM, TO 200Å.	Al(4, 6): Cp = 211/211, Gp = 0.5/57, ±5 = -3.65/-2.95 = 0.7, ±10 = -4.9/-2.84 = 2.06, ±20 = -7.0/-0.2 = 6.8;Al(5, 5): Cp = 55/193, Gp = 8/50, ±5 = 0.4, ±10 = 1.76, ±20 = 6.0;g(CC): Cp = 127/121, Gp = 10/22, ±5 = -2.85/-0.4 = 2.45, ±10 = -3.9/0.1 = 4.0, ±20 = -3.56/-0.2 = 3.36;Hg(ES): Cp = 156/155, Gp = 239/57, ±5 = -4.15/-2.05, = 2.1, ±10 = -5.38/-1.0 = 4.38, ±20 = -5.52/-0.2 = 5.32.	
FME-12;PGO-1-1	100Å TOX/400Å NITRIDE, 0 RPM.	Al(4, 12): Cp = 54/59, Gp = 15/8, ±10&±20&±50 NO FERROELECTRIC Al(8, 11): Cp = 65/75, Gp = 17/13, ±10&±20 NO FERROELECTRIC Hg(C): Cp = 62/69, Gp = 8/8, ±10&±20 NO FERROELECTRIC WINDOW	
FME-21;BT0-18-5	470°C/30 MIN., 10 mTORR, 0 RPM	Al(6, 2): Cp = 122/175, Gp = 30/54, ±5 = 0, ±10 = 2.1, ±20 = 6.2 Al(6, 3): Cp = 96/176, Gp = 23/62, ±5 = 0.2, ±10 = 1.1, ±20 = 6.8 Hg(C): Cp = 88/84, Gp = 29/26, ±5 = 0, ±10 = 2.6, ±20 = 6.4 Hg(CC): Cp = 77/80, Gp = 41/48, ±5 = 0, ±10 = 2.7, ±20 = 7.2	
FMMF-013;BMF-Si-185	G.T. = 150°C, RTA 600°C, 10 SEC., IN $H2/N_2$, 270 nM AT CENTER	Al(9, 10): Cp = 108/101, Gp = 14/56, ±5 = 1.12/3.0 = 1.88, ±10 = -0.1/3.5 = 3.4, ±20 = -1.2/10.8 = 12.0, Al(8, 8): Cp = 114/107, Gp = 16/63, ±5 = 0.85/2.65 = 1.8, ±10 = -0.5/3.44 = 3.94, ±20 = -2.88/9.2 = 12.08, Hg(CC): Cp = 88/85, Gp = 25/43, ±5 = -1.6/3.52 = 5.12, ±10 = -3.62/4.44 = 8.06, ±20 = BROKE DOWN, Hg(ES): Cp = 106/102, Gp = 34/61, ±5 = -1.72/ 2.95 = 4.67, ±10 = -3.32/4.24 = 7.48, ±20 = -14.8/6.48 = 21.28	
FMF-09;BTO-19-1	100Å TO/200Å NIT., 450°C/30 MIN., 50 mTORR, 0 RPM	Al(5, 2): Cp = 209/209, Gp = 0.5/52, ±5 = -3.6/-2.15 = 1.45, ±10 = -4.36/-1.36 = 3.0, ±20 = -2.4/2.88 = 5.28, Al(5, 3): Cp = 185/185, Gp = 54/92, ±5 = -3.25/-2.2 = 1.05, ±10 = -3.8/-1.5 = 2.3, ±20 = -1.0/2.36 = 3.36, Al(4, 2): Cp = 203/202, Gp = 28/61, ±10 = -3.56/-0.72 = 2.84.	LASER FOCUS PROBLEM.

Wafer #	Experiment	Test Results	Comments
FMF-10;BTO-19-2	100Å TO/200Å NIT., 450°C/30 MIN., 50 mTORR, 0 RPM.	Al(15/14): Cp = 240/240, Gp = 55/101, ±5 = -4.25/-3.78 = 0.47, ±10 = -4.7/-3.4 = 1.3, ±20 = BK DOWN, Al(16, 16): Cp = 207/206, Gp = 48/80, ±5 = -3.48/-1.75 = 1.73, ±10 = -3.96/-0.74 = 3.22. Hg(C): Cp = 77/68, Gp = 6/11, ±5 = -2.7/-1.05 = 1.65, ±10 = -3.44/ -0.56 = 2.88, ±20 = -0.6/3.8 = 4.4, Hg(E): Cp = 172/171, Gp = 37/57, ±5 = -2.8/-2.3 = 0.5, ±10 = -3.8/-1.3 = 2.5, ±20 = -5.2/2.6 = 7.8.	
FMF-11;BTO-19-3	100ÅTO/200ÅNIT., 450°C/30 MIN. 50mTORR, 0 RPM	Al(5, 3): Cp = 214/213, Gp = 46/80, ±5 = -3.8/-1.9 = 1.9, ±10 = -2.36/-0.8 = 1.56, ±20 = -1.72/3.8 = 5.52, Al(4, 2): Cp = 220/219, Gp = 54/92, ±5 = -4.05/-2.2 = 1.85, ±10 = -5.36/-1.24 = 4.12, ±20 = -2.88/3.6 = 6.48, Hg(A): Cp = 120/112, Gp = 12/20, ±5 = -2.4/-1.3 = 1.1, ±10 = -2.7/-0.84 = 1.86, ±20 = -0.4/2.4 = 2.8, Hg(B): Cp = 143/139, Gp = 17/28, ±5 = -2.05/-1.38 = 0.67, ±10 = -2.3/-1.1 = 1.2, ±20 = BK DOWN.	
FMF-12;BTO-19-4	100ÅTO/200Å NIT., 550°C/30 MIN., 50 mTORR, 0 RPM.	Al(13, 17): Cp = 382/380, Gp = 65/192, ±5 = 0.25, ±10 = -2.1/-1.2 = 0.9, ±20 = BROKE DOWN, Al(11, 14): Cp = 421/421, Gp = 239/239, ±5 = -2.6/-2.1 = 0.5, ±10 = -2.84/-1.6 = 1.24, ±20 = BK DOWN, Hg(1R): Cp = 270/152, Gp = 84/38, ±5 = -2.55/-0.95 = 1.6, ±10 = -2.8/-0.3 = 2.5, ±20 = BK DOWN, Hg(2R): Cp = 117/117, Gp = 61/52, ±5 = -1.3/0.3 = 1.6, ±10 = -1.86/-0.2 = 1.66, ±20 = -1.12/0.2 = 1.32.	
FMF-16;PGO-2-1	100ÅTO/200ÅNIT., RT, 50mTORR, 30 MIN., 0 RPM, FURNANCE ANEAL	Hg(R): Cp = 44/51, Gp = 16/9, ±10 = 0.6, ±20 = -9.28/-8.2 = 1.0	
FMF-17;PGO-2-2	100ÅTO/200Å NIT., RT, 50 mTORR, 30 MIN., 0 RPM, RTA	Hg(R): Cp = 61/66, Gp = 13/46, ±5 = -2.8/-2.62 = 0.18, ±10 = -3.0/-2.56 = 0.44, ±20 = -6.8/-0.64 = 6.16	
FMF-18;PZTO-2-1	100ÅTO/200ÅNIT. 550°C/30 MIN. 300 mTORR, 0 RPM	Al(3, 3): Cp = 114/114, Gp = 22/49, ±5 = 0.4/1.7 = 1.3, ±10 = 0.56/1.5 = 0.94, ±20 = SONOS; Al(2, 2): Cp = 101/100, Gp = 19/34, ±5 = 0.52/1.88 = 1.36, ±10 = 0.8/1.7 = 0.9,. ±20 = SONOS, Hg(A): Cp = 45/43, Gp = 3/9, ±5 = -1.3/3.0 = 4.3, ±10 = -2.56/4.6 = 6.66, ±20 = SONOS; Hg(B): Cp = 50/48, Gp = 4/8, ±5 = 0.45/4.1 = 3.65, ±10 = -2.1/4.5 = 6.6, ±20 = 2.88/4.2 = 1.32.	
FMF-19;PZT-2-2	100Å TO/200 NIT. 550°C/40 MIN. 300 mTORR, 0 RPM	Al(10/15): Cp = 60/46, Gp = 12/23, ±10 = 0, ±20 = 0; Al(9, 9): Cp = 82/56, Gp = 26/24, ±10 = 0.2, ±20 = 0.2; Hg(A): Cp = 37/31, Gp = 8/12, ±5 = 0, ±10 = 3, ±20 = 3, Hg(B): Cp = 59/49, Gp = 35/27, ±5 = 0, ±10 = 1.2, ±20 = 3.2.	
FME-22;BTO-19-5	550°C/30 MIN., 200 mTORR, 0 RPM	Al(5, 3): Cp = 273/271, Gp = 59/132, ±5 = -1.7/-0.85 = 0.85, ±10 = -2.1/-0.4 = 1.7, ±20 = 0.2/1.28 = 1.48. Al(4, 5): Cp = 272/284, Gp = 312/138, ±5 = -3.6/-3.22 = 0.38, ±10 = -4.2/-2.98 = 1.22, ±20 = BROKE DOWN, Hg(1R): Cp = 162/157, Gp = 176/190, ±5 = -1.5/0.15 = 1.65, ±10 = -1.84/0.4 = 2 24, ±20 = -0.72/2.08 = 2.8, Hg(2R): Cp = 63/156, Gp = 11/38, ±5 = 1.4, ±10 = 3, ±20 = BROKE DOWN.	
FME-23;BTO-20-1	550°C/40 MIN. 10 mTORR, 0 RPM	Hg(C): Cp = 189/187, Gp = 143/173, ±5 = -1.5/-1.3 = 0.2; ±10 = -3.0/ -1.24 = 1.76; ±20 = SONOS	
FME-24;LBTO-3-1	550°C/40 MIN., 50 mTORR, 0 RPM	Al(10, 16): Cp = 311/310, Gp = 28/116, ±5 = -2.38/-1.48 = 0.9, ±10 = -2.8/-0.76 = 2.04, ±10 = -2.8/-0.76 = 2.04, ±20 = -2/4.4 = 6.4, Al(9, 13): Cp = 361/361, Gp = 44/164, ±5 = -2.15/-1.5 = 0.65, ±10 = -2.8/-0.76 = 2.04, ±20 = -2/4 5 = 6.5, Hg(1R): Cp = 102/100, Gp = 25/31, ±5 = -2.4/-0.35 = 2.05, ±10 = -2.64/0.3 = 2.94, ±20 = BROKE DOWN, Hg(2R): Cp = 111/108, Gp = 93/98, ±5 = -2 55/-0.62 = 1.93, ±10 = -4.6/0.44 = 5.04, ±20 = -7.56/4.08 = 11.64; AFTER 400°C/1 Hr. BAKE 250mTORR O_2: Al(10, 13): Cp = 311/308, Gp = 30/114, ±10 = -2.6/2.2 = 4.8, Hg(1R): Cp = 151/244, Gp = 31/205, ±10 = -2.8/1.8 = 4.6, Hg(2R): Cp = 83/83, Gp = 7/14, ±10 = -3 1/1.1 = 4.3.	
FMF-5;LBTO-3-2	100ÅTO/200ÅNIT., 550°C, 50mTORR, 0 RPM.	Al(10, 15), Cp = 175/175, Gp = 72/74; ±10 WINDOW = 0; Al(10, 9); Cp = 218/218, Gp = 174, ±10 WINDOW = 0. Hg(1R); Cp = 111/111, Gp = 12/20, ±5 = -3.7/-1.92 = 1.78, ±10 = -4.92/-1.0 = 3.92, ±20 = -9.04/1.6 = 10.64	
FAMFF-10, 3; LBTO-3-3	200Å TO, 559°C, 50mTORR, LONG DEP. 0 RPM.	Al(6, 5): Cp = 112/112, Gp = 48/46, ±10 WINDOW = 0; Al(5, 5): Cp = 124/124, Gp = 53/53, ±10 WINDOW = 0.	

Wafer #	Experiment	Test Results	Comments
FMF-6;BTO-20-2 / CJYBCO-1B	450°C/40 MIN., 200mTORR, 0 RPM , SUPER COND. 550°C/30 MIN 0 RPM	Sent Back To STC	
FMF-7;LBTO-3-4 YBCO	450°C/2 Hr(5Hz), 100ÅTO/200Å NIT, 200mTORR, 0 RPM .	Sent Back To STC	
FMF-08;BTO-20-3	100ÅTO/200ÅNIT., 450°C/2Hr., 5Hz., 200mTORR, 0 RPM.	Al(15, 10): Cp = 238/238, Gp = 95/95, ±20 Window = 0; Al(11, 10): Cp = 218/218, Gp = 74/74, ±20 = Window = 0.	
FMG-02;BTO-20-4	450°C/2Hr., 5Hz., 200mTORR, 0 RPM	Al(5, 6): Cp = 271/271, Gp = 114/114, ±20 Window = 0; Al(7, 8): Cp = 252/252, Gp = 100/100, ±20 Window = 0	
FMG-01;LBTO-2-1	450°C/2Hr., 5Hz., 200mTORR, 0 RPM	Al(6, 4): Cp = 158/158, Gp = 37/37, ±20 Window = 0; Al(4, 5): Cp = 176/176, Gp = 50/50, ±20 Window = 0.	
FMF-20;BTO-21-3	YTTRIUM BUFFER-YSZ-1-1;450°C/ 20 MIN., 10 Hz, 0 RPM, 5E-4 O_2, BTO 450°C/25 MIN., 10 Hz, O RPM, 5E-4 O_2.	INDIUM DOTS ON TOP BTO HAD HIGH CONDUCTIVITY; ±2 VOLTS ≈0.1 V WINDOW	
FMF-23;LBTO-1-1	450°C/40 MIN., 200 mTORR, ITO DOTS ON LBTO, 0 RPM.	ITO(3, 4): Cp = 185/174, Gp = 1034/1006, ±5 = 0/0.43, ±10 = -0.2/0.64 = 0.84, ±20 = 0.8/2.36 = 1.56; ITO(3, 6): Cp = 210/201, Gp = 1257/1218, ±5 = -0.2/0.35 = 0.55, ±10 = -0.4/0.5 = 0.9, ±20 = 1.0/2.8 = 1.8; Hg(1R): Cp = 275/264, Gp = 576/619, ±5 = -, ±10≈0.1, ±20 = BROKE DOWN, Hg(2R): Cp = 202/198, Gp = 99/133, ±5≈0.1, ±10≈0.2, ±20 = SONOS, Hg(OR): Cp = 347/327, Gp = 496/554, ±5≈0.1, ±10≈0.2, ±20 = SONOS.	
FMF-24;LBTO-1-2	450°C/40 MIN., 50mTORR, 0 RPM, ITO DOTS.	ITO(4, 5): Cp = 183/189, Gp = 1223/1203, ±5≈0, ±10≈0, ±20≈0, ITO(3, 3): Cp = 285/275, Gp = 677/706 ±5≈0, ±10≈0, ±20≈0. Hg(1R): Cp = 487/452, Gp = 1520/1589, ±5≈0, ±10≈0, ±20≈0. Hg(OR): Cp = 130/129, Gp = 62/79, ±5≈0, ±10≈0.1, ±20≈0.2.	
FMF-25;LBTO-1-3	450°C/66MIN., 50mTORR, 10Hz, 0 RPM, TiW 700Å DOTS ON LBTO	TiW(5, 4): Cp = 275/263, Gp = 1078/1098, ±10 = 0, ±20 = 0; TiW(3, 6): Cp = 189/177, Gp = 1587/1551, ±10 = 0, ±20 = 0; Hg(OR): Cp = 153/151, Gp = 176/195, ±10 = 0, ±20 = 0; Hg(3R): Cp = 164/162, Gp = 61/83, ±10 = 0, ±20 = 0;	
FMG-3;BTO-21-2 / PGO-2-3	BTO 450°/5 MIN. 200 mTORR, 0 RPM		
FMG-4;BTO-21-2	R.T./40 MIN. 200mTORR, 10Hz, 0 RPM	Hg(G);Cp = 12.6, ±20≈2.0, Hg(E); Cp = 19, ±20≈1.4, Hg(B); Cp = 13.7, ±20≈1.4.	
FMG-12;LBTO-2-4	450°C/40 MIN. 10Hz, 50 mTORR, 0 RPM		
FMG-1X;BTO-21-4 (FMG-25)	450°C/30 MIN., 200mTORR, 10Hz, 0 RPM	Hg(R);Cp = 201.4, ±10≈2.45, Hg(Q); Cp = 200.4, ±5≈1.8, Hg(N); Cp = 202.3, ±20≈2.4, Hg(L); Cp = 146.6, ±10≈11, Hg(K); Cp = 144.8, ±5≈1.8, Hg(E);Cp = 146, ±20≈14.8, Hg(D); Cp = 223.3, ±5≈1.68, Hg(C); Cp = 225.3, Hg(B); Cp = 225, ±20≈2.9.	
FMG-3X;BTO-21-6	450°C/30 MIN., 50mTORR, 10Hz, 0 RPM	Hg(F);Cp = 488, ±10≈0.45, Hg(E);Cp = 395, ±20≈0.8, Hg9C); Cp = 293, ±10≈0.3, Hg(A);Cp = 290, ±20≈0.7.	
FMF-22;LBTO-2-3	450°C/40MIN., 50mTORR, 0 RPM, 1400Å TiW DOTS ON LBTO	TiW(3, 4): Cp = 490/460, Gp = 1005/1155, ±10 = 0, ±20 = 0, TiW(2, 4): Cp = 637/599, Gp = 850/1139, ±10 = 0, ±20 = 0 Hg(1R): Cp = 344/332, Gp = 652/782, ±10 = 0, ±20 = 0; Hg(2R): Cp = 432/412, Gp = 652/782, ±10 = 0, ±20 = 0;	
FMG-13;LBTO-1-4	550°C/30MIN., 200mTORR, 0 RPM, 600Å QUARTZ CAP (SPUTTERED)	Hg(1R): Cp = 103/103, Gp = 16/27, ±5 = 1.32/2.08 = 0.76, ±10 = 1.06/2.2 = 1.14, ±20 = 1.4/3.52 = 2.12, Hg(2R): Cp = 97/96, Gp = 16/25, ±5 = 1.25/1.92 = 0.67, ±10 = 1.1/2.2 = 1.1, ±20 = 0.8/3.12 = 2.32;	
FMG-2X;BTO-21-5	450°C/30MIN., 50mTORR, 0 RPM, 600Å QUARTZ CAP	Hg(1R): Cp = 213/210, Gp = 158/205, ±5≈0.2, ±10≈0.1, ±20≈0.2. Hg(2R): Cp = 148/148, Gp = 66/108, ±5 = 0.5/0.65 = 0.15, ±10 = 0.5/0.9 = 0.4, ±20≈0.'	
FMG-5X;LBTO-2-5	550°C/30MIN., 200mTORR, 0 RPM, 200Å OX BUFFER.....AFTER 600Å SPUTTERED QUARTZ CAP	NO CAP: Hg(C);Cp = 151/150, Gp = 16/37; ±5 = -3.22/2.58 = 5.8, ±10 = -2.2/3.2 = 5.4, ±20 = BOOKE DOWN; Hg(1R);Cp = 239/233, Gp = 173/227, ±5 = -0.65/0.1 = 0.75, ±10 = -0.65/0.45 = 0.4, ±20 = BROKE DOWN;-------CAPPED: Hg(CC);Cp = 89/89, Gp = 35/18, ±5 = -1.1/0.35 = 0.75, ±10 = -1.2/0 = 1.2, ±20 = 1.0/1.88 = 0.88, Hg(R);Cp = 114/114, Gp = 16/29, ±5 = -1.68/-0.38 = 1.3, ±10 = -1.84/0 = 1.84, ±20 = -1.0/1.0 = 2.0.	

Wafer #	Experiment	Test Results	Comments
FMG-4X;BTO-21-7	450°C/30 MIN., 50 mTORR, 0 RPM	Hg(C); Cp = 152/147, Gp = 77/98, ±5 = -0.78/3.05 = 3.83; ±10 = 0.6/2.01 = 1.41; ±20 = SONOS; Hg(1R); Cp = 312/298, Gp = 633/689, ±5 = 0, ±10 = SONOS.	
PENN. ST. BTO ON Si		NO OBSERVABLE HYSTERESIS	
PENN. ST. BTO ON NITRIDE		Hg(L); Cp = 166.5, ±10 = 0.6, Hg(A); Cp = 180, ±20 = 5.6.	
PENN. ST. PGO ON Si LG-31		Hg(A); Cp = 34.36/36.27, Gp = 2.3/4.5, ±5 = 2.6, ±10 = 5.6, ±20 = 7.8, AFTER ANNEAL 500°C/2Hr. 250 mTORR OX. Hg(AA);Cp = 70.84/65.17, Gp = 20/17, ±5 = 0, ±10 = 5.5, ±20 = 8.8	
PENN. ST. PGO ON Si LG-32		Hg(G);±50 = 25, Hg(F);Cp = 32.42, ±42 = 22.5, Hg(E);Cp = 32.22, ±35 = 17.5, Hg(D);Cp = 31.53, ±20 = 8.5, Hg(C);Cp = 30.32, ±10 = 3.6 ANNEAL 500°C/2Hr. 250mTORR OX. Cp = 45.64/42.15, Gp = 14/8, ±5 = 0, ±10 = 1.9, ±20 = SONOS.	
PENN. ST. PGO ON Si LG-33		NO OBSERVABLE HYSTERESIS	
PENN. ST. PGO ON Si LG-34		Hg(E);Cp = 39.72, ±50 = 4, Hg(C);±50 = 6.1	
FMG-6X; BTO-22-1	550°C/30MIN. 200mTORR, 0 RPM.	Hg(C); Cp = 184/120, Gp = 246/342, ±5 = 6.1, ±10 = 2.1/8.8 = 6.7, ±20 = SONOS; Hg(1R); Cp = 207/198, Gp = 255/355, ±5 = 0, ±10 = SONOS	
FMF-21; LBTO-2-2	550°C/40MIN. 50mTORR, 0 RPM	Hg(C); Cp+529/507, Gp = 401/622, ±5 = 0.62/0.9 = 0.28, ±10 = 0.4/0.96 = 0.56, ±20 = 2/3.2 = 1.2; Hg(1R); Cp = 208/205, Gp = 16/56, ±5 = 0.15/0.52 = 0.37, ±10 = 0/0.76 = 0.76, ±20 = BROKE DOWN.	
FMG-14; LBTO-1-5	550°C/33MIN. 200mTORR, 0 RPM, BUFFER Ox/NITRIDE OXIDIZED	Hg(1R); Cp = 292/285, Gp = 515/562, ±5 = 0.25, ±10 = 0.5, ±20 = 1.0/1.92 = 0.92, Hg(C); Cp = 459/457, Gp = 351/478, ±5 = 0.3, ±10 = -1.6/-1.06 = 0.54, ±20 = 1.0/2.52 = 1.52.	
FMG-15; NBTO-1-1	OX/NIT. BUFFER, 550°C/30 MIN. 200 mTORR, 0 RPM.; TiW Dots Deposited Through Mask	Hg(C);Cp = 146/146, Gp = 14/29, ±5 = -0.93/0.07 = 1.0, ±10 = -1.24/0.36 = 1.6, ±20 = 0.2/2.6 = 2.4; Hg(R); Cp = 186/185, Gp = 90/119, ±5 = -0.88/-0.28 = 0.6, ±10 = -1.1/0.05 = 1.15, ±20 = 1.0/2.6 = 1.6. TiW(6, 8);Cp = 705/632, Gp = 778/1498, ±5 = -0.55/-0.1 = 0.45, ±10 = -0.8/0.2 = 1.0; TiW(6, 7); Cp = 596/570, Gp = 668/889, ±5 = -0.5/0.2 = 0.7, ±10 = -0.8/0.64 = 1.44, ±20 = -0.48/2.2 = 2.68	
FMG-16; NOPZT-1-1	R.T./30 MIN, 200mTORR, 0 RPM, RTA 650°C/10 SEC O_2.	Hg(C); Cp = 14/13, Gp = 0/1.4, ±5 = 7.2, ±10 = 14, ±20 = -0.2/19.2 = 19.4, Hg(1R); Cp = 14/13, Gp = 0.7/1.1, ±5 = 8.6, ±10 = -3.3/9.5 = 12.8, ±20 = BROKE DOWN	
FMG-17; NOPZT-1-2	550°C/30 MIN, 300 mTORR, 0 RPM	Hg(C); Cp = 36/29, Gp = 6.7/14.3, ±5 = 1, ±10 = -2.6/7.1 = 9.7, ±20 = BROKE DOWN; Hg(1R); Cp = 66/62, Gp = 10/44, ±5 = -0.95/1.1 = 2.05, ±10 = -1.5/3.6 = 5.1, ±20 = -0.2/4.6 = 4.8	
FMG-18; NBTO-1-2	550°C40 MIN, 200mTORR, 20 RPM QUARTZ CAP = 624Å, TiW DOTS-1620Å	Hg(C); Cp = 275/269, Gp = 365/912, ±5 = 0.3, ±10 = 0.6, ±20 = BROKE DOWN, ; Hg(EN); Cp = 161/159, Gp = 14/39, ±5 = 0.15, ±10 = 1.0, ±20 = SONOS. TiW(3, 6), Cp = 274/271, Gp = 135/190, ±5 = 0.49/1.61, ±10 = 0.5/1.9 = 1.4, ±20 = 1.6/3.52 = 1.92; TiW(7, 9); Cp = 385/380, Gp = 341/400, ±5 = -3.38/-2.58 = 0.8, ±10 = -3.44/2.16 = 1.28, ±20 = -2.2/-0.2 = 2.0.	
FMG-19;NBTO-1-3	550°C/20 MIN, 200mTORR, 20RPM, 30Hz	Hg(EN); Cp = 193/191, Gp = 46/82, ±5 = -0.2/0.7 = 0.9, ±10 = 0.2/0.7 = 0.5, ±20 = BROKE DOWN; Hg(EEN); Cp = 187/184, Gp = 76/103, ±5 = -0.75/0.48 = 1.23, ±10 = -0.9/0.6 = 1.5, ±20 = -0.2/2.08 = 2.28.	
07X;NBTO-2-1	550°C/40MIN, 200mTORR, 20RPM, 10 Hz, BUFF. = 200Å TO.	Hg(C); Cp = 250/271, Gp = 904/1562, ±5 = -0.1/0.1 = 0.2, ±10 = 0.05/0.76 = 0.71, ±20 = BROKE DOWN, Hg(EN); Cp = 602/561, Gp = 339/705, ±5 = 0.2, ±10 = -1.0/-0.64 = 0.36, ±20 = BROKE DOWN	
FMG-20;NPZT-1-3	R.T./15MIN. 200mTORR, 0RPM, 10Hz, RTA 650°C/10SEC.	Hg(C); Cp = 41/41, Gp = 0.3/15, ±5 = 1.75, ±10 = 1.3/3.8 = 2.5, ±20 = SONOS; Hg(1R); Cp = 50/49, Gp = 4/6, ±5 = 2.4, ±10 = 2/4.6 = 2.6, ±20 = BROKE DOWN.	
7869-1;NBTO-2-2	550°C/40MIN. 200mTORR, 20RPM, 10Hz.		
7869-2;NBTO-2-3	BUFF.OX/NIT/OXIDATION; 500°C/60MIN., 200mTORR, 20RPM, 10Hz.		

Appendix C: Westinghouse 8K FERRAM Test Vehicle Design Description

The 6083 FERRAM maskset consists of four different designs incorporating ferroelectric technology. These four designs are the 6081, 6082, 6084, and 6085 chips. the 6081 chip is the 8K SONOS EEPROM designed by Sandia National Labs (SNL) and successfully built at ATL as the 6071 chip. The 6082 and 6084 chips are the SNL test pattern chip and the Westinghouse- designed test pattern chip, respectively. They were also included on the 6073 maskset as the 6072 and 6074 chips. The 6085 is a SNL-designed test chip consisting of various "SELF-STRESSING" circuits.

The modifications to the 6071, 6072, and 6074 designs consisted mainly of "Biteching" to the new process/ mask layer sequence, and changing the appropriate SONOS-ferroelectric-related layers in the memory devices as well as adding Via and Metal-2 to the designs (the original 4μM SONOS process is a single level metal process). On the 6081 chip, the only modifications made were in the core memory array, where it was necessary to change the poly-memory-gate shapes to Metal-1, and add Via and Metal-2. The following pages describe the design rules, projection plate composition, and contents of the test chips.

C.1 Sandia Design Rules Extracted from "SA3776 DWG" (CALMA L6070)

1) 1.0 P-well
a) min. width . . . . . 22 um
b) min. space . . . . . 26 um
c) rec. space to L2 . . . . . 1 um; butting OK
d) space to L6 . . . . . 19 um

2) 2.0 P+ G.B.
a) min. width . . . . . 4 um
b) min. space . . . . . 16 um

3) 3.0 Thin oxide cut (device window)
a) min. width . . . . . 8 um
b) min. space (n+) . . . . . 8 um
c) min. space (p+) . . . . . 12 um

4) 4.0 Poly 1
a) min. width . . . . . 4 um
b) min. space . . . . . 4 um
c) overlap of L3 (n-ch) . . . . . 0 um
d) overlap of L3 (p-ch) . . . . . 4 um

5) 5.0 N- implant (extended-drain)
a) min. width . . . . . 8 um
b) overlap of L4 (channel length direction) . . . . . 2 um

6) 6.0 P+ implant

a) min. width	8 um
b) min. space	8 um
c) overlap of L3	3 um

7) 7.0 Contact window

a) min. width	3 um
b) min. space	4 um
c) enclosed by L4	2.5 um
d) enclosed by L15	3 um
e) enclosed by L6	2.5 um
f) enclosed by L16	2.5 um
g) space to L4	2.5 um
h) enclosed by L3	2 um
i) enclosed by L8	0.5 um

8) 8.0 Metal

a) min. width	4 um
b) min. space	4 um

9) 9.0 Bond pad etch

a) enclosed by L8	4 um

10) 12.0 Memory gate

a) overlap of L16 (channel width direction)	3.75 um
b) overlap of L15	4 um

11) 15.0 Poly 2

same as for poly 1 (4a-d)

12) 16.0 N+ implant

a) min. width	8 um
b) min. space	8 um
c) space to L2	4 um

13) 18.0 Poly 2 stringer etch

a) min. space	4 um
b) overlap of L15	2 um
c) space to L4	2 um

14) 23.0 Field adjust implant

a) min. space	4 um
b) overlap of L3 (p-ch)	5 um
c) overlap of L1	11 um

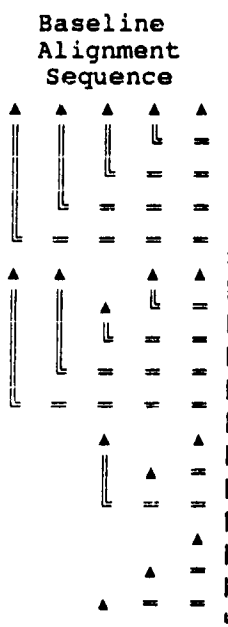
C.2 Westinghouse 4 um FE/SONOS/CMOS CALMA and Mask Levels for Ferroelectric Version of Sandia EEPROMs. (Calma Libraries L6080, L6081, L6082, L6084)

WEC CALMA	Fill Code	Mask Level	Mask Polarity	Description
0	NA	0.0	Clear	Alignment
† 1	12	1.0	Clear	N-well
2	16	2.0	Clear	P-well
3	NA	3.0	Opaque	N+ Guard band
4	71	4.0	Clear	P+ Guard band
5	11	5.0	Opaque	Device window
6	104	6.0	Opaque	Non-mem poly
7	5	7.0	Clear	N- implant
8	NA	8.0	Clear	N+ implant
9	90	9.0	Clear	P+ implant
*10	10	10.0	Clear	Contact
11	91	11.0	Clear	Memory window
12	83	12.0	Opaque	FE removal
*13	76	13.0	Opaque	Metal 1
14	96	14.0	Clear	Via
*15	NA	15.0	Opaque	Metal 2
16	82	16.0	Clear	Overcoat

† The N-well layer (L1) is generated by DRC program.

* DRC sizing required.

C.3 Alignment Tolerances



L#	Level Name	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	Alignment		1	1	1	1	1	2	2	3	2	2	3	4	3	4	5	6
1	N-Well			2	2	2	2	3	3	4	3	3	4	5	4	5	6	7
2	P-Well				2	2	2	3	3	4	3	3	4	5	4	5	6	7
3	N+ G.B.					2	2	3	3	4	3	3	4	5	4	5	6	7
4	P+ G.B.						2	3	3	4	3	3	4	5	4	5	6	7
5	Dev. Window							1	1	2	1	1	2	3	2	3	4	5
6	Poly								2	3	2	2	3	4	3	4	5	6
7	N-Implant									3	2	2	3	4	3	4	5	6
8	N+Implant										3	3	4	5	4	5	6	7
	P+Implant											2	3	4	3	4	5	6
10	Contact												1	2	1	2	3	4
11	Mem.Window													1	2	3	4	5
12	F.E.Removal														3	4	5	6
13	Metal 1															1	2	3
14	Via																1	2
15	Metal 2																	
16	Overcoat																	

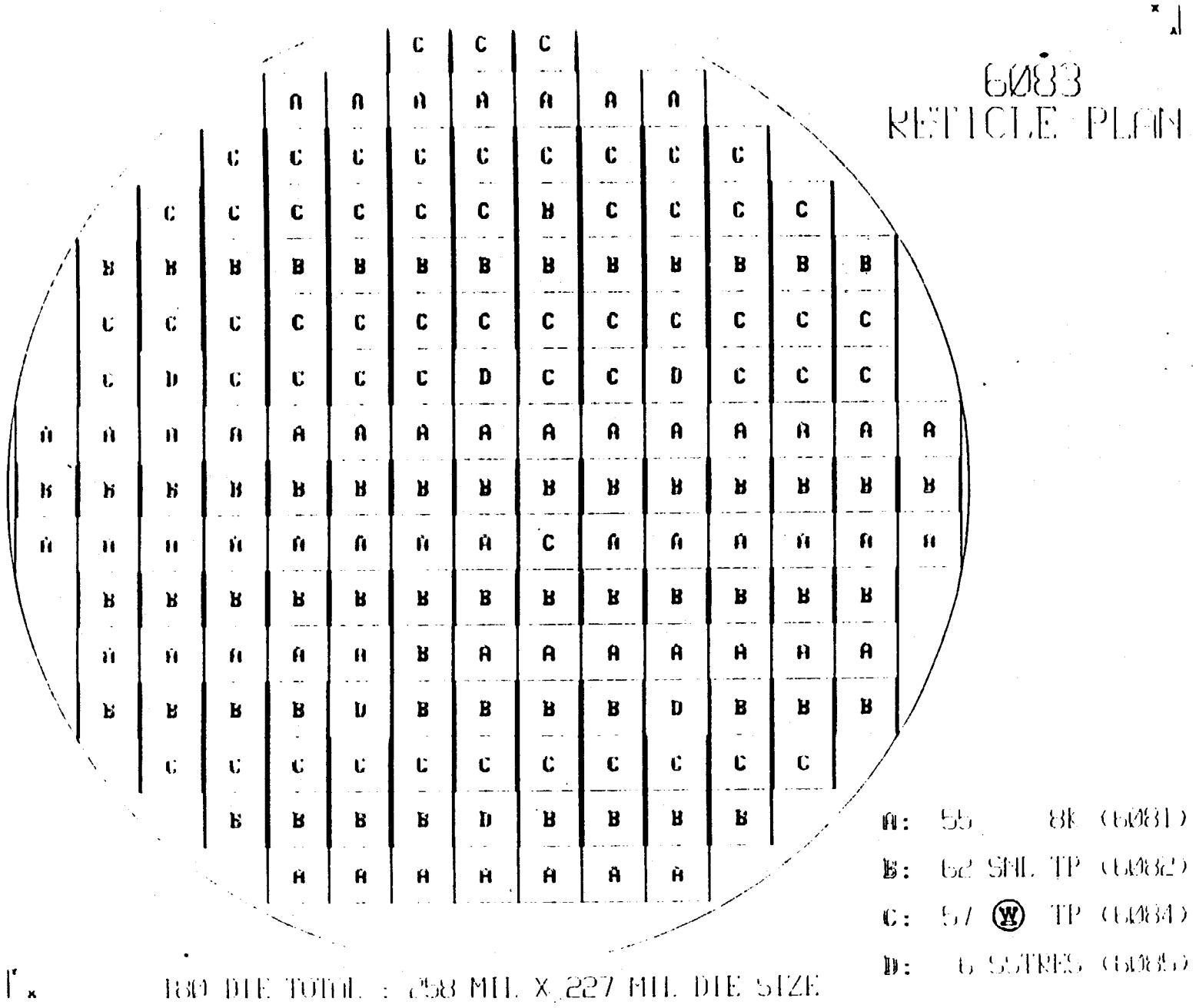


Figure C-1: FERRAM ICAL Test Vehicle Reticle Plan

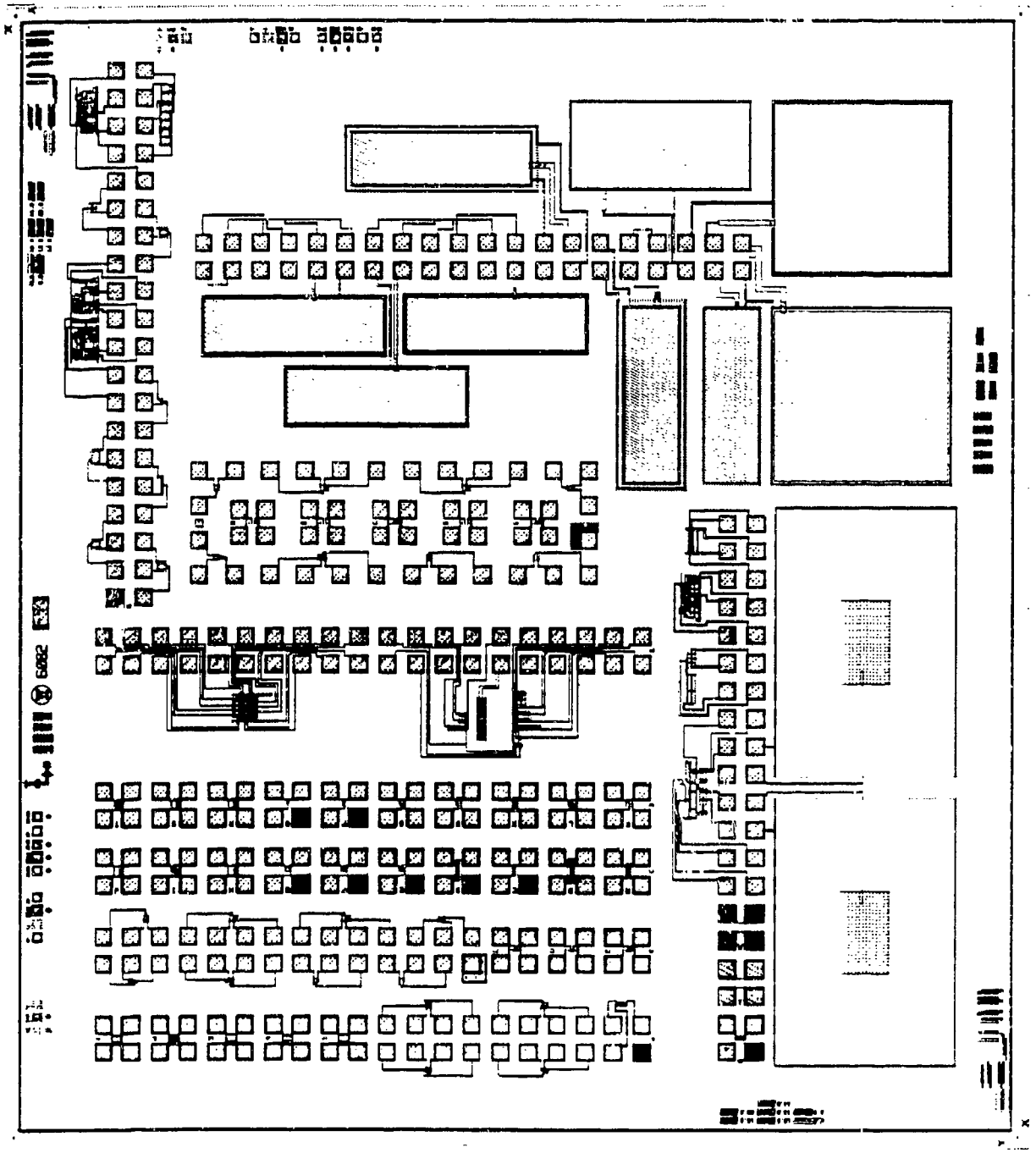


Figure C-2: The 6082 FERRAM/SNL ICAL Test Chip

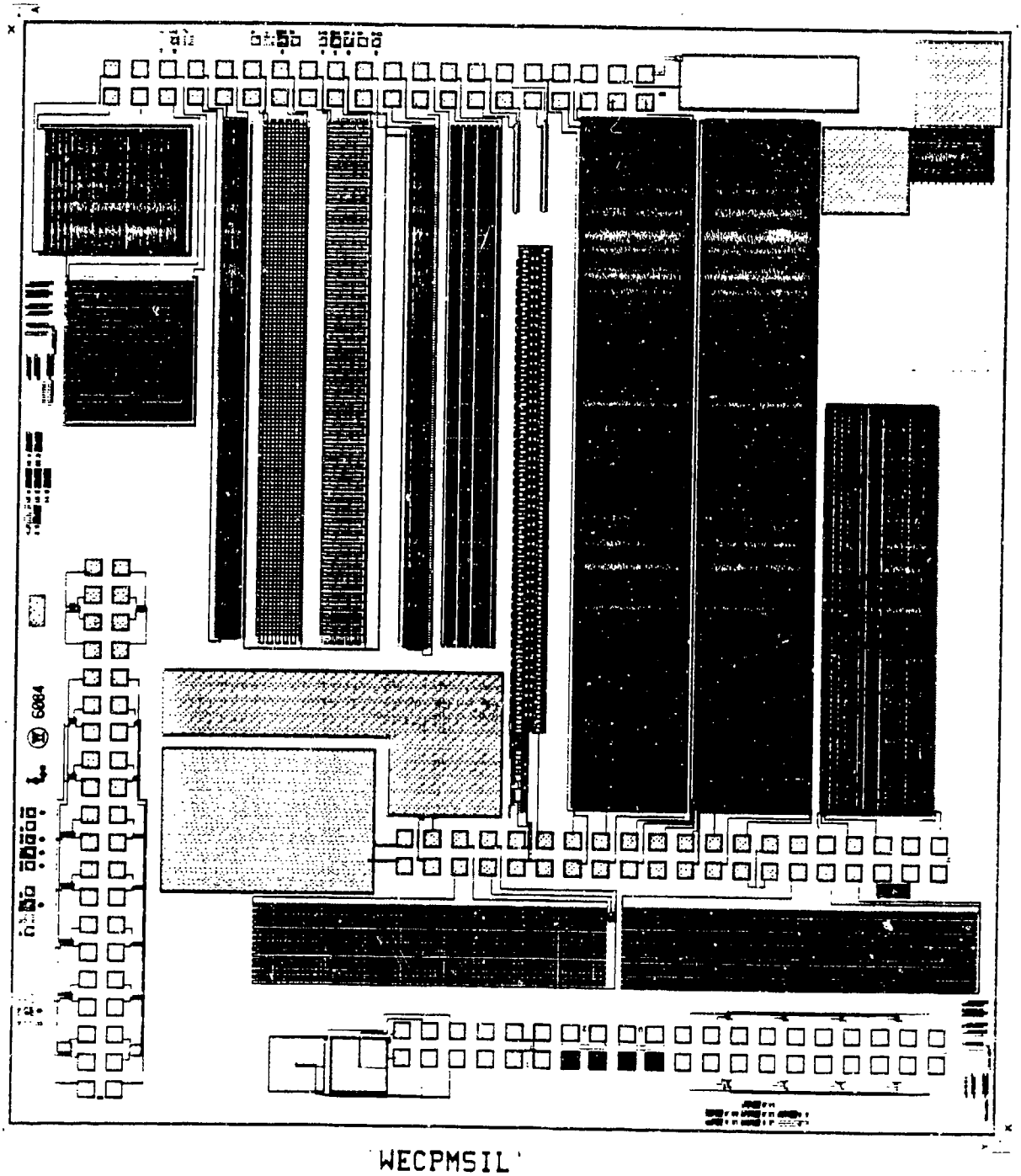


Figure C-3: The 6084 FERRAM/WEC ICAL Test Chip

C.4 Description of "TA751_ATL" 4 μm FENV/CMOS Test Chip

CALMA Library : L6082
CALMA Structure : TA751_ATL

Following is a listing of test structures included in the nine padsets:

(1) TP13_ATLP

This padset consists of SNL Module-13 structures (eight 8/4 FENV transistors) and also SCR structures C, D, and E (Tx= 13, 10, and 8 μm, respectively). See figures 1-1 and 1-2.

FENV pinouts (one pin for source and P-well)

Source	Gate	Drain	P-well
20	18	19	20
23	21	22	23
13	11	12	13
10	8	9	10
34	32	33	34

FENV pinouts (separate pins for source and P-well)

Source	Gate	Drain	P-well
16	14	15	17
26	24	25	27
30	28	29	31

N-substrate pin 7

SCR C:	N-sub 5	P+ 6	P-well 36	N+ 35
SCR D:	N-sub 3	P+ 4	P-well 38	N+ 37
SCR E:	N-sub 1	P+ 2	P-well 40	N+ 39

(2) RESIST_CAP_ATLP

This padset consists of the six SNL capacitors (A, B, C, D, E, and F), poly Van der Pauw (pins 27-32... see figure 10), metal Van der Pauw (pins 21- 26), N+ resistor (pins 19, 20), P+ resistor (pins 36, 37), and the current mirror circuit.

A. Capacitor A is a metal gate capacitor in p-well with P+/P+ GB under gate. Its area is 0.5 x 10^6 μm^2. (Pins 4,3).

B. Capacitor B is a metal gate capacitor in p-well with P+/P+ GB under gate. Its area is 0.3 x 10^6 μm^2. (Pins 4,5,6 P-well).

C. Capacitor C is a metal gate capacitor in p-well with P+ GB under gate and a P+ halo around gate. Its area is 0.3 x 10^6 μm^2. (Pins 34,33,7 P-well).

D. Capacitor D is a poly 1 capacitor in a blanket p-well and guardband substrate with P+ halo. Its area is 0.3 x 10^6 μm^2. (Pins 2,1).

E. Capacitor E is a poly 1 capacitor in p-well with P+ halo. Its area is 1.0 x 10^6 μm^2. (Pins 40,1).

F. Capacitor F is a poly 1 capacitor in n-well with N+ halo. Its area is 1.0 x 10^6 μm^2. (Pins 39,38).

(3) A_TO_J_ATLP

This padset consists of SNL transistors A to J (ten total).

A. An NMOS transistor with W/L of 40/4 (C4810_CEL).

source 2 gate 40 drain 39 P-well 1

B. An NMOS transistor with W/L of 100/10 (C4820_CEL).

source 4 gate 38 drain 37 P-well 3

C. A PMOS transistor with W/L of 40/4 (C4830_CEL).

source 6 gate 36 drain 35 N-sub 5

D. A PMOS transistor with W/L of 100/10 (C4840_CEL).

source 8 gate 34 drain 33 N-sub 7

E. A PMOS poly field oxide transistor with W/L of 22/14 (C4850 CEL).

source 10 gate 32 drain 31 N-sub 9

F. A PMOS metal field oxide transistor with W/L of 22/14 (N+ GB under gate) (C4860_CEL).

source 12 gate 30 drain 29 P-well 11

G. A PMOS metal field oxide transistor with W/L of 22/14 (no N+ GB under gate) (C4910_CEL).

source 14 gate 28 drain 27 N-sub 13

H. An NMOS metal gate transistor with W/L of 26/18 (no GB under gate) (C4920_CEL).

source 16 gate 26 drain 25 P-well 15

I. An NMOS poly transistor with W/L of 26/18 (no GB under gate). (C4930_CEL).

source 18 gate 24 drain 23 P-well 17

J. An NMOS metal gate transistor with W/L of 26/18 (GB under gate). (C4940_CEL).

source 20 gate 22 drain 21 P-well 19

(4) K_TO_T_ATLP

This padset consists of SNL transistors K to T (ten total).

K. An N-FENV transistor with W/L of 8/4 (C4950_CEL).

P-well 1 source 2 drain 39 gate 40

L. An NMOS poly field oxide transistor with W/L of 26/18 (no GB under gate) (C4960_CEL).

P-well 3 source 4 drain 37 gate 38

M. An NMOS N-extender transistor with W/L of 40/4. This transistor differs from A in that the area of the source and drain is larger. Space from oxide to poly is 11 microns instead of 8 microns(C5010_CEL).

source 6 gate 36 drain 35 P-well 5

N. An NMOS N-extender transistor with W/L of 30/3 (C5020_CEL).

P-well 7 source 8 gate 34 drain 33

O. An NMOS N-extender transistor with W/L of 20/2 (C5030_CEL).

P-well 9 source 10 gate 32 drain 31

P. A PMOS transistor with W/L of 30/3 (C5040_CEL).

N-sub 11 source 12 gate 30 drain 29

Q. A PMOS transistor with W/L of 20/2 (C5050_CEL).

N-sub 13 source 14 gate 28 drain 27

R. An NMOS metal field oxide transistor with W/L of 26/18 (no GB under gate) (C5060_CEL).

P-well 15 source 16 gate 26 drain 25

S. An NMOS metal field oxide transistor with W/L of 26/18 (GB under gate) (C5070_CEL).

P-well 17 source 18 gate 24 drain 23

T. An NMOS poly field oxide transistor with W/L of 26/18 (GB under gate) (C5080_CEL).

P-well 19 source 20 gate 22 drain 21

(5) C3542C_ATLP

The following structures are included:

* analog cell C
* exploded CM5X_CEL (from analog cell B)
* exploded TRIGGER_CEL (from analog cell B)
* n-channel transistor (from analog cell A)
* N- implant only transistor (from analog cell B)

a) 18/30 N- implant only:	source 6	gate 8	drain 7
b) 7/11 P+ xtr:	source 12	gate 14	drain 13
c) 7/90 P+ xtr:	source 15	gate 17	drain 16
d) 9/30 N- implant only:	source 18	gate 20	drain 19
e) 18/30 N- implant only:	source 24	gate 22	drain 23
f) 18/60 N- implant only:	source 27	gate 25	drain 26
g) 10/30 NMOS:	source 36	gate 34	drain 35

N-sub 21

(6) DIODES_ATLP

This padset consists of the following:

* C2210C_CEL (p-channel 40/4 metal transistor with no memory cut)
  N-sub 20 source 19 gate 21 drain 22
* N+ to P-well diode
  N+ 10 P-well 9
* P+ to N-sub diode
  P+ 11 N-sub 12
* Metal Van der Pauw (structure Y)
  pins 17, 18, 23, 24
* Poly Van der Pauw (structure W)
  pins 15, 16, 25, 26
* INV_CEL (from analog cell A)
* CM5X_CEL (from analog cell A)
* LSHIFT_CEL (from analog cell A)
* TRIGGER_CEL (from analog cell A)

(7) TP3_9_ATLP

This padset includes SNL Module 3 (small memory array) and Module 9 (n and p-channel transistors): Module 3 is a 4 row by 3 bit memory array. The schematic for Module 3 is shown in figure 7-1. It contains a "dummy" row as can be found in the SA2999, SA3612, and SA3182. In this case, however, both the MNOS and NMOS gates are tied to the p-well, whereas in the actual array it is just the MNOS gates. The sizes, in microns, of the transistors are shown in parentheses. The width of the transistor is shown before the '_' whereas the length of the transistor follows the '_'. The alpha character is the transistor type; P for P-channel, N for N-channel.

	Drain	Gate	Source	P-well
8/2.4 N-FENV	9	10	31	36
8/4 NMOS	3	37	31	36
100/10 NMOS	2	37	31	36
50/5 NMOS	1	37	31	36
40/4 NMOS	40	37	31	36
2 series				
4/16 NMOS	39	37	31	36
4/16 NMOS	38	37	31	36

	Drain	Gate	Source	N-sub
100/10 PMOS	32	35	31	6
40/4 PMOS	34	35	31	6
40/4 PMOS	33	35	31	6
with 2x drain contact-to-gate space				

(8) TP14_ATLP

This has the same structures as SNL Module 14 except for two fewer of transistors C2210A_CEL and C2210_CEL, it also includes transistors 1-5 below. See figure 8.

1. An NMOS poly gate oxide transistor with W/L of 26/26 (GB under gate) (C5081_CEL).
   source 21 gate 19 drain 22 P-well 20
2. An NMOS metal field oxide transistor with W/L of 26/18 (GB under gate) (C5082_CEL).
   source 23 gate 17 drain 24 P-well 18
3. An N-FENV metal gate oxide transistor with W/L of 26/20.6 (GB under gate) (C5083_CEL).
   source 25 gate 15 drain 26 P-well 16
4. An NMOS metal gate oxide transistor with W/L of 26/20.6 (GB under gate) (C5084_CEL).
   source 27 gate 13 drain 28 P-well 14
5. An N-FENV metal gate oxide transistor with W/L of 26/26 (no GB under gate) (C5085_CEL).
   source 29 gate 11 drain 30 P-well 12

FENV N-channel transistors

source	gate	drain	P-well
8	10	9	7
33	31	32	34
4	6	5	3
37	35	36	38

FENV P-channel transistors

source	gate	drain	N-sub
40	2	39	1

(9) C2200_CEL

This is kept exactly as SNL Module 13, it is NOT padded out to 2x20 padset per SNL's request. TP13 ATLP is the Westinghouse-testable version of this Module.

C.5 Description of L6084 " WECPM_ATL" 4 μm FENV/CMOS Test Chip

List of structures placed in L6084 "WECPM_ATL":

1) M_POL_CWSTR_ATL : a metal to poly contact string consisting of 4800 3μm X 3μm
(padset A) contacts (pins 4,5), and tap for 160 contacts (pins 5,6)

2) M_NPL_CWSTR_ATL : a metal to N+ contact string consisting of 4800
(padset A) 3 μm X 3 μm contacts (pins 23, 24), and a tap for 160 contacts (pins 18, 23). P-well contact is pin 17.

3) M_POL_RSCT_ATLP : a poly resolution/continuity structure consisting of vertical
(padset A) poly serpentine inside poly comb (LW-4μm, LS-4μM) over horizontal device window stripes (LW-8μm, LS-8μM) over P-well with P-well contact.
poly combs : pins 36, 38
poly serp : pins 37, 39
P-well : pin 40

4) MOVERP_RSCT_ATL : a metal over poly resin/cont structure consisting of vertical
(padset A) metal serpentine inside comb (LW-4μm, LS-4μm) over horizontal poly serp/comb (LW-4μm, LS-4μm)
poly serp : pins 12, 33
poly combs : pins 29, 30
metal serp : pins 9, 10
metal combs : pins 31, 32

5) M_RSCT_NOM_ATL : a vertical metal serp/comb structure (LW-4μm, LS-4μm)
(padset A) metal serp : pins 13, 14
metal combs : pins 27, 28

6) DCHAIN_ATL : a gate delay chain consisting of 100 inverter gates
(padset A) (Wp-32μm, Wn-15μm)
in 26 out 16 vdd 15 vss 25

7) MODEL_XTRS_ATLP : various sized NMOS and PMOS transistors for modeling
(padset B) purposes, common source and common substrate connected 50x50, 50x5, 50x4, 50x3, 50x2, 12x4, 8x4

NMOS

W/L	G	D
50/50	22	23
50/5	24	25
50/4	26	27

PMOS

W/L	G	D
50/50	19	18
50/5	17	16
50/4	15	14

50/3	28	29	50/3	13	12
50/2	30	31	50/2	11	10
12/4	32	33	12/4	9	8
8/4	34	35	8/4	7	6
source 36			source 5		
P-well 21			N-sub 20		

*40/4 NMOS annular transistor:
source 40 drain 39 gate 38 P-well 37

*40/4 PMOS annular transistor:
source 1 drain 2 gate 3 N-sub 4

8) SONOS_XTRS_ATLP (padset C) : various sized N-FENV transistors, common source and common substrate connected:
10x5, 10x4, 10x3, 10x2
a P+, an N+, a Poly, and a Metal 1 Kelvin contact a 26x26 PMOS transistor with N+ G.B. under gate

N-FENV			P-FENV		
W/L	G	D	W/L	G	D
10/5	2	3	10/5	39	38
10/4	4	5	10/4	37	36
10/3	6	7	10/3	35	34
10/2	8	9	10/2	33	32
source 10			source 31		
P-well 1			N-sub 40		

* P+ : pins 11, 12
M1 : pins 30, 29

* poly : pins 13, 14
M1 : pins 28, 27

* M2 : pins 15, 16
M1 : pins 26, 25

* N+ : pins 17, 18
M1 : pins 24, 23

* 26/26 PMOS : source 20 gate 22 drain 21 N-sub 19

9) SRP_ATL : spreading resistance probe structure (N-well, P-well, N+G.B. P+ G.B., N-implant, N+implant, P+implant; all 125μm x 800μm

10) JC_TBS : TBS structure (a 25 x 25 array of 8μmx4μm PMOS transistors)

11) JC_VERTNPN : a vertical NPN device
(padset A) N-sub : pin 7
P-well : pin 8
N+ : pin 34

12) JC_MPCAP : a 1000μmx1000μm poly (pin 21)
(padset A) to metal one (pin 20) capacitor.